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A CMOS Clock Recovery Circuit for 2.5-Gb/s NRZ Data

Seema Butala Anand and Behzad Razavi, *Member, IEEE*

***Abstract*—This paper describes a phase-locked clock recovery circuit that operates at 2.5 Gb/s in a 0.4-μm digital CMOS technology. To achieve a high speed with low power dissipation, a two-stage ring oscillator is introduced that employs an excess phase technique to operate reliably across a wide range. A sample-and-hold phase detector is also described that combines the advantages of linear and nonlinear phase detectors. The recovered clock exhibits an rms jitter of 10.8 ps for a PRBS sequence of length $2^7 - 1$ and a phase noise of -80 dBc/Hz at a 5-MHz offset. The core circuit dissipates a total power of 33.5 mW from a 3.3-V supply and occupies an area of 0.8×0.4 mm^2.**

***Index Terms*—Clock and data recovery, optical communication, oscillators, phase detectors, PLLs.**

I. Introduction

THE rapid increase of real-time audio and video transport over the Internet has led to a global demand for high-speed serial-data communication networks. To accommodate the required bandwidth, an increasing number of wide-area networks (WANs) and local-area networks (LANs) are converting the transmission medium from a copper wire to fiber. This trend motivates research on low-cost, low-power integrated fiber-optic receivers. A critical task in such receivers is the recovery of the clock embedded in the nonreturn-to-zero (NRZ) serial-data stream. The recovered clock both removes the jitter and distortion in the data and retimes it for further processing.

This paper describes the design and implementation of a phase-locked CMOS clock recovery circuit that employs a number of novel techniques to support a data rate of 2.5 Gb/s. A two-stage ring oscillator incorporating an excess phase shift method achieves a high speed, enabling reliable operation in a 0.4-μm CMOS technology. In addition, a phase detection technique based on an analog sample-and-hold circuit is introduced that exhibits a high speed while producing a small ripple on the control voltage of the oscillator. Measurements on the fabricated prototype indicate an rms jitter of 10.8 ps for a pseudorandom bit sequence (PRBS) of $2^7 - 1$. The circuit dissipates 33.5 mW from a 3.3-V supply and occupies an area of 0.8×0.4 mm^2.

The next section of the paper presents the clock recovery architecture and design issues. Section III describes the building blocks and Section IV summarizes the experimental results.

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The authors are with the Electrical Engineering Department, University of California at Los Angeles, Los Angeles, CA 90095–1594 USA (e-mail: razavi@icsl.ucla.edu).

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II. Architecture

Two properties of NRZ data make clock recovery difficult. First, arbitrarily long consecutive sequences of 1s or 0s limit the capture range of the phase-locked loop and allow the oscillation frequency to drift. Second, NRZ data contains no spectral content at the bit rate, requiring edge detection. These properties impact the choice of the clock recovery architecture: 1) in the absence of data transitions in the input bit sequence, the phase detector must not generate any false phase comparisons and 2) the circuit requires a nonlinear operation to create a spectral line at the bit rate.

Clock recovery circuits designed for WANs such as SONET or SDH require a narrow-loop bandwidth to meet the jitter transfer specification. This in turn severely limits the capture range of a simple phase-locked loop. For this reason, a means of frequency detection is also necessary so as to guarantee lock in the presence of large oscillator frequency variations.

In addition to the above issues, various sources of jitter affect the design of the overall system as well. In clock recovery circuits, five sources of jitter can be identified: 1) jitter generated from a noisy input; 2) oscillator jitter due to device electronic noise; 3) supply and substrate noise; 4) disturbance of oscillator by leakage of data transitions through the phase detector; and 5) oscillator jitter due to ripple on the control line.

The effect of input jitter is reduced by a narrow-loop bandwidth and the oscillator jitter is lowered through the use of large swings and careful design with respect to phase noise. All of the building blocks are fully differential so as to minimize the effect of supply and common-mode noise. Moreover, a buffer isolates the oscillator from the data transitions coupled through the phase detector.

At low supply voltages, the VCO gain K_{VCO} required to achieve a given tuning range becomes quite large. As a result, the ripple on the control voltage due to the phase detector activity creates greater jitter at the output. The conflict between a wide tuning range and a low VCO sensitivity is resolved by a provision for two control inputs, a fine control driven by the main loop and a coarse control that will be driven by a frequency-locked loop (FFL) in future implementations. Since the FLL remains relatively quiet (or can be disabled) after phase lock, the high sensitivity of coarse control does not lead to high jitter.

The architecture of the clock recovery circuit addressing the above issues is shown in Fig. 1. The loop consists of a phase detector (PD), a voltage-to-current (V/I) converter, a passive loop filter, and a ring-based voltage-controlled oscillator (VCO). The VCO provides the main output through a set of open-drain buffers to 50-Ω termination resistors.

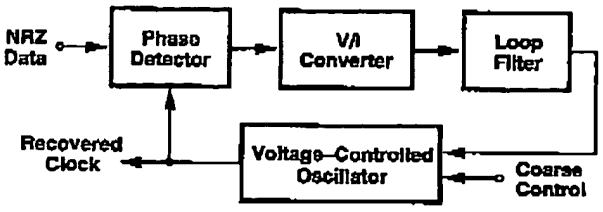

Fig. 1. PLL architecture.

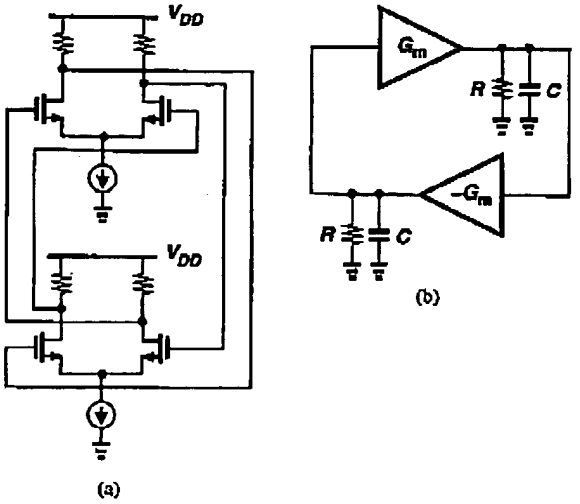

Fig. 2. (a) Two-stage ring oscillator. (b) Simplified model of (a).

Designing the circuit to operate at 2.5 GHz in a 0.4-μm CMOS technology entails a number of challenges. The next section will deal with the design of each building block.

III. Building Blocks

In this section, the transistor-level implementation of each building block is described, emphasizing the design constraints imposed by the technology limitations.

A. VCO

Since the clock recovery circuit is designed with the provision of adding a frequency detector, the oscillator must generate quadrature outputs [1], [2]. For a differential ring oscillator, this observation dictates the need for an even number of stages. In the 0.4-μm CMOS technology used here, the maximum oscillation frequency does not exceed 1.8 GHz for a four-stage ring (and 2.4 GHz for a three-stage ring). Thus, to achieve reliable operation at 2.5 GHz, a two-stage topology is necessary. However, two simple differential pairs in a loop [Fig. 2(a)] fail to oscillate because each stage contributes only one pole, yielding insufficient phase at unity gain. The simplified model shown in Fig. 2(b) illustrates this effect. The total frequency-dependent phase shift around the loop reaches 180° only at infinite frequency, where the loop gain drops to zero. Thus, excess phase must be introduced in each stage [3], [4].

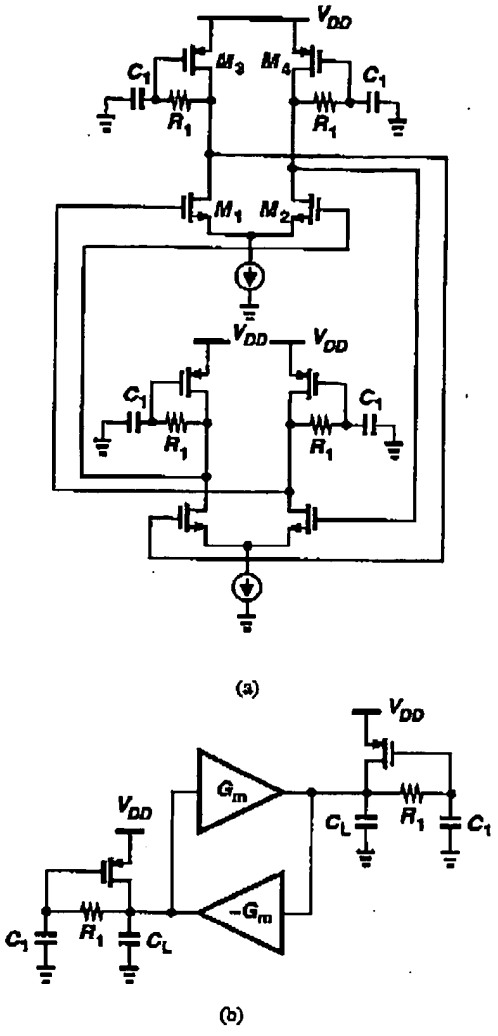

Fig. 3. (a) Two-stage ring oscillator with a composite load. (b) Simplified model of (a).

In Fig. 3(a), the load resistors are replaced with a composite load consisting of R_1, C_1, and a pMOS device. With the proper choice of parameters, such a load is inductive and can provide enough phase shift to allow oscillation. The model shown in Fig. 3(b) can be used to study the behavior of the oscillator. Note that, in addition to C_1, each stage contains a load capacitance C_L, which represents the drain junction capacitance of the MOS devices, the input capacitance of the next stage, and the input capacitances of the isolation buffers.

At this point, it is necessary to determine the parameters of the composite load so as to ensure oscillation. We obtain the transfer function for the half circuit equivalent of each differential pair as

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}(1 + R_1 C_1 s)}{g_{m3} + (C_1 + C_L + R_1 C_1/r_{o3})s + R_1 C_1 C_L s^2}.$$

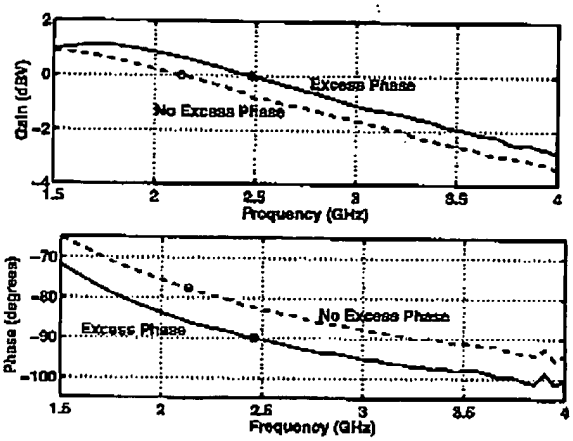

Fig. 4. Gain and phase response of each delay stage.

The circuit exhibits a zero at $-1/R_1C_1$ and two poles whose sum is given by

$$\omega_{p1} + \omega_{p2} = \frac{C_1 + C_L}{R_1 C_1 C_L}$$

where channel-length modulation is neglected.

Oscillation of the two-stage VCO depends on careful placement of the poles and the zero, with a requisite 90° phase shift at the unity-gain frequency ω_u for each stage. This in turn mandates that each pole frequency be less than the frequency of the zero. Hence,

$$\frac{C_1 + C_L}{R_1 C_1 C_L} < \frac{2}{R_1 C_1}$$

and consequently

$$C_1 < C_L.$$

The above condition can be easily met by the proper choice of device dimensions.

Fig. 4 plots the simulated gain and phase of each stage as a function of frequency with and without the excess phase network. Two important points can be observed: 1) the unity-gain frequency is *higher* with the R_1-C_1 network due to the inductive behavior of the load and 2) the circuit satisfies Barkhausen's oscillation criteria at a single frequency ($\approx$ 2.5 GHz) in the presence of R_1 and C_1 but falls short by 13° (per stage) at ω_u without the excess phase network. Note that R_1 is actually a pMOS device operating in the deep triode region, with its gate bypassed to V_{DD} to minimize the effect of common-mode noise.

The phase noise due to the thermal noise of resistors R_1 in Fig. 3(b) is of concern. To quantify the phase noise, a small sinusoid is placed in series with one of the resistors [Fig. 5(a)], the oscillator is simulated in the time domain, and the output spectrum is examined. With proper normalization, the phase noise from the additional resistors can be determined for a given frequency offset. Fig. 5(b) shows the output spectrum for a 5-mV_p sinusoidal source. This result indicates that, after normalization

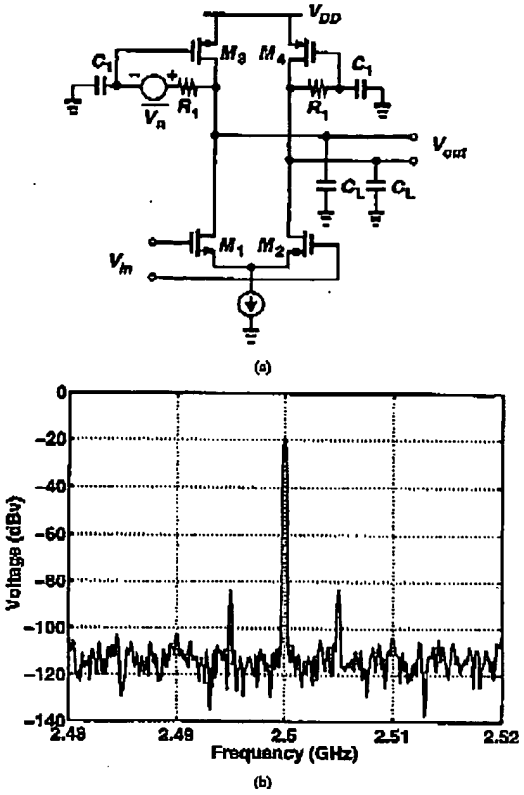

Fig. 5. (a) One stage of a VCO with noise due to R_1. (b) Output spectrum of a VCO with noise tone.

to the actual noise value ($4kTR_1$), the total phase noise due to all four resistors in the VCO is roughly equal to -143.2 dBc/Hz at a 5-MHz offset, a value much less than the contribution of the other devices.

In order to vary the oscillation frequency, the VCO incorporates delay interpolation [5], providing a tuning range wide enough to encompass process and temperature variations [Fig. 6(a)]. In the transistor implementation of each delay stage, shown in Fig. 6(b), the fast path consists of one differential pair, M_1-M_2, whereas the slow path consists of two differential pairs, M_5-M_6 and M_7-M_8. Interpolation is accomplished by varying the tail currents of M_1-M_2 and M_7-M_8 in opposite directions.

The fast and slow paths share the load consisting of M_3-M_4 and the R_1-C_1 networks. Since the limited voltage headroom makes it difficult to control the currents of M_1-M_2 and M_7-M_8 by another differential pair, transistors M_9 and M_{10} are driven by a current folding circuit (Fig. 7). Setting the gain of both paths, both M_9 and M_{10} in fact consist of smaller transistors, a narrow transistor and a wide one, so as to provide fine and coarse tuning.

An interesting phenomenon in the interpolating VCO topology used here is its relatively linear input–output characteristic. This property arises because two effects *cancel* each other: the nonlinearity associated with the voltage-to-current conversion in the pMOS differential pairs (M_{1c}-M_{2c} and

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PATENT

ANALOG FRONT-END HAVING BUILT-IN EQUALIZATION AND APPLICATIONS THEREOF

BACKGROUND OF THE INVENTION

TECHNICAL FIELD OF THE INVENTION

[0001] This invention relates generally to communication systems and more particularly to an enhanced data conveyance within such communication systems.

DESCRIPTION OF RELATED ART

[0002] Communication systems are known to transport large amounts of data between a plurality of end user devices. Such end user devices include telephones, facsimile machines, computers, television sets, cellular phones, personal digital assistants, et cetera. As is also known, such communication systems may be a local area network (LAN) and/or a wide area network (WAN). A local area network is generally understood to be a network that interconnects a plurality of end user devices distributed over a localized area (e.g., up to a radius of 10 kilometers) and includes LAN infrastructure equipment. For example, a local area network may be used to interconnect workstations distributed within an office of a single building or a group of buildings, to interconnect computer based equipment distributed around a factory or hospital, et cetera. As is further known, local area networks may be wired local area networks or wireless local area networks. Wired local area networks typically have a star topology, ring topology, bus topology or hub/tree topology.

[0003] A wide area network is generally understood to be a network that covers a wide geographic area and includes WAN infrastructure equipment. Wide area networks include both public data networks and enterprise wide private data networks. A public data network is established and operated by a national network administrator specifically for data transmission. Such public data networks facilitate the inner

working of equipment from different manufacturers. Accordingly, standardizations by the ITU-T have been established for conveying data within public data networks. Currently, there are two main types of public data networks: packet switched public data networks and circuit switched public data networks. For example, the public switched telephone network is a circuit switched public data network while the Internet is a packet switched public data network. Other examples of wide area networks include integrated service digital networks (ISDN) and broadband multiservice networks.

[0004] As is further known, communication systems may be networked together to yield larger communication systems, where such networking is typically referred to as internetworking. Internetworking is achieved via internetworking units that allow communication networks using the same or different protocols to be linked together. The internetworking units may be routers, gateways, protocol converters, bridges, and/or switches.

[0005] Regardless of the type of communication system (e.g., LAN, WAN, or internetworking system), each communication system employs a data conveyance protocol to ensure that data is accurately conveyed within the system. In general, a protocol is a formal set of rules and conventions that govern how system devices (i.e., end user devices, LAN infrastructure equipment, WAN infrastructure equipment, and/or internetworking units) exchange data within the communication system. Such protocols typically include regulations on receiver sensitivity (i.e., how noisy a received signal may be and how small its amplitude may be) for signals received by a system device or within a system device and on transmit power of a signal from one system device to another or within the system device.

[0006] As is further known, each system device processes millions of bits of data per second. Accordingly, each system device includes high-speed data interfaces to

efficiently input and output data. Such interfaces are typically implemented as integrated circuits that are mounted on a printed circuit board. A group of printed circuit boards may be mounted on a back plane and multiple back planes may further be placed in a rack to make up the system device.

[0007] In an effort to meet the ever-increasing challenges of improving data conveyance speed, each system device includes an increasing number of integrated circuits, printed circuit boards (PCBs), and/or racks. Typically, the racks and PCB's are coupled together using coaxial cables, fiber optics, connectors, and/or wires. The integrated circuits on a printed circuit board are operably coupled together via copper traces (e.g., FR4 connections). As the number and complexity of the system devices increases, along with the desired speed of conveying data therebetween, the distance between ICs, PCBs, and/or racks is increasing in diversity. Some communication channels between ICs, PCBs, and/or racks may be relatively short (i.e., have a channel response that introduces minimal distortion of the signals it carries) while others are relatively long (i.e., have a channel response that introduces significant distortion of the signals it carries).

[0008] Typically, a receiver section of a high-speed data interface includes an equalizer to compensate for the distortion produced as a result of the channel response. Typically, the equalizer is set to compensate for the channel response of a nominal channel. In other words, the equalizer is fixed to provide a nominal equalization response, which corresponds to the inverse of the nominal channel response. However, as the channel responses vary more and more due to the increasing diversity of channel lengths, a fixed equalizer is inadequate to meet the receiver sensitivity requirements of many standardized protocols.

[0009] Therefore, a need exists for programmable equalizer for use within receiver sections of high-speed data interfaces.

BRIEF SUMMARY OF THE INVENTION

[0010] The analog front-end having built-in equalization of the present invention substantially meets these needs and others. In one embodiment, an analog front-end having built-in equalization includes a control module and a tunable gain stage. The control module is operably coupled to provide a frequency response setting based on a channel response of a channel providing high-speed serial data to the analog front-end. The tunable gain stage includes a frequency dependent load and an amplifier input section. The frequency dependent load is adjusted based on the frequency response setting. The amplifier input section is operably coupled to the frequency dependent load and receives the high-speed serial data. In conjunction with the frequency dependent load, the amplifier input section amplifies and equalizes the high-speed serial data to produce an amplified and equalized serial data. As such, an analog front-end may have its built-in equalizer adjusted to compensate for the varying channel responses.

[0011] In another embodiment, an analog front-end having built-in equalization includes a frequency dependent load, and amplifier input section. The amplifier input section is operably coupled to the frequency dependent load and receives high-speed serial data. In conjunction with the frequency dependent load, the amplifier input section amplifies and equalizes the high-speed serial data to produce an amplified and equalized serial data.

[0012] Such an analog front-end having built-in equalization may be incorporated in a high-speed data receiver that receives high-speed serial data via a channel. The channel may be of varying lengths and as such have varying channel responses. Based on the channel response,

the analog front-end is adjusted to provide an appropriate level of equalization.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0013] Figure 1 is a schematic block diagram of a programmable logic device in accordance with the present invention;

[0014] Figure 2 is a schematic block diagram of a programmable multi-gigabit transceiver in accordance with the present invention;

[0015] Figure 3 is a schematic block diagram of a programmable receive physical media attachment (PMA) module in accordance with the present invention;

[0016] Figure 4 is a schematic block diagram of a programmable front-end in accordance with the present invention;

[0017] Figure 5 is a schematic block diagram of an alternate embodiment of a programmable front-end in accordance with the present invention;

[0018] Figures 6 and 6A are schematic block diagrams of various embodiments of a tunable gain stage in accordance with the present invention;

[0019] Figure 7 is a schematic block diagram of an alternate embodiment of a tunable gain stage in accordance with the present invention; and

[0020] Figures 8A-8D illustrate various channels, channel responses and programmable equalization in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0021] Figure 1 is a schematic block diagram of a programmable logic device 10 that includes programmable logic fabric 12, a plurality of programmable multi-gigabit transceivers (PMGT) 14-28 and a control module 30. The programmable logic device 10 may be a programmable logic

array device, a programmable array logic device, an erasable programmable logic device, and/or a field programmable gate array (FPGA). When the programmable logic device 10 is a field programmable gate array (FPGA), the programmable logic fabric 12 may be implemented as a symmetric array configuration, a row-based configuration, a sea-of-gates configuration, and/or a hierarchical programmable logic device configuration. The programmable logic fabric 12 may further include at least one dedicated fixed processor, such as a microprocessor core, to further facilitate the programmable flexibility offered by a programmable logic device 10.

[0022] The control module 30 may be contained within the programmable logic fabric 12 or it may be a separate module. In either implementation, the control module 30 generates the control signals to program each of the transmit and receive sections of the programmable multi-gigabit transceivers 14-28. In general, each of the programmable multi-gigabit transceivers 14-28 performs a serial-to-parallel conversion on received data and performs a parallel-to-serial conversion on transmit data. The parallel data may be 8-bits, 16-bits, 32-bits, 64-bits, et cetera wide. Typically, the serial data will be a 1-bit stream of data that may be a binary level signal, multi-level signal, etc. Further, two or more programmable multi-gigabit transceivers may be bonded together to provide greater transmitting speeds. For example, if multi-gigabit transceivers 14, 16 and 18 are transceiving data at 3.125 gigabits-per-second, the transceivers 14-18 may be bonded together such that the effective serial rate is 3 times 3.125 gigabits-per-second.

[0023] Each of the programmable multi-gigabit transceivers 14-28 may be individually programmed to conform to separate standards. In addition, the transmit path and receive path of each multi-gigabit transceiver 14-28 may be separately programmed such that the transmit path of a transceiver is supporting one standard while the receive path of the same

transceiver is supporting a different standard. Further, the serial rates of the transmit path and receive path may be programmed from 1 gigabit-per-second to tens of gigabits-per-second. The size of the parallel data in the transmit and receive sections, or paths, is also programmable and may vary from 8-bits, 16-bits, 32-bits, 64-bits, et cetera.

[0024] Figure 2 is a schematic block diagram of one embodiment of a representative one of the programmable multi-gigabit transceivers 14-28. As shown, the programmable multi-gigabit transceiver includes a programmable physical media attachment (PMA) module 32, a programmable physical coding sub-layer (PCS) module 34, a programmable interface 36, a control module 35, a PMA memory mapping register 45 and a PCS register 56. The control module 35, based on the desired mode of operation for the individual programmable multi-gigabit transceiver 14-28, generates a programmed deserialization setting 66, a programmed serialization setting 64, a receive PMA_PCS interface setting 62, a transmit PMA_PCS interface setting 60, and a logic interface setting 58. The control module 35 may be a separate device within each of the multi-gigabit transceivers and/or included within the control module 30. In either embodiment of the PMGT control module 35, the programmable logic device control module 30 determines the corresponding overall desired operating conditions for the programmable logic device 10 and provides the corresponding operating parameters for a given multi-gigabit transceiver to its control module 35, which generates the settings 58-66.

[0025] The programmable physical media attachment (PMA) module 32 includes a programmable transmit PMA module 38 and a programmable receive PMA module 40. The programmable transmit PMA module 38 is operably coupled to convert transmit parallel data 48 into transmit serial data 50 in accordance with the programmed serialization setting 64. The programmed serialization setting 64 indicates the desired rate of the transmit serial data 50, the desired rate of the

transmit parallel data 48, and the data width of the transmit parallel data 48. The programmable receive PMA module 40, which will be described in greater detail with reference to Figure 3, is operably coupled to convert receive serial data 52 into receive parallel data 54 based on the programmed deserialization setting 66. The programmed deserialization setting 66 indicates the rate of the receive serial data 52, the desired rate of the receive parallel data 54, and the data width of the receive parallel data 54. The PMA memory mapping register 45 may store the serialization setting 64 and the deserialization setting 66.

[0026] The programmable physical coding sub-layer (PCS) module 34 includes a programmable transmit PCS module 42 and a programmable receive PCS module 44. The programmable transmit PCS module 42 receives transmit data words 46 from the programmable logic fabric 12 via the programmable interface 36 and converts them into the transmit parallel data 48 in accordance with the transmit PMA_PCS interface setting 60. The transmit PMA_PCS interface setting 60 indicates the rate of the transmit data words 46, the size of the transmit data words (e.g., 1-byte, 2-bytes, 3-bytes, 4-bytes, et cetera) and the corresponding transmission rate of the transmit parallel data 48. The programmable receive PCS module 44 converts the received parallel data 54 into received data words 56 in accordance with the receive PMA_PCS interface setting 62. The received PMA_PCS interface setting 62 indicates the rate at which the received parallel data 54 will be received, the width of the parallel data 54, the transmit rate of the received data words 56 and the word size of the received data words 56.

[0027] The control module 35 also generates the logic interface setting 58 that provides the rates at which the transmit data words 46 and receive data words 56 will be transceived with the programmable logic fabric 12. Note that the transmit data words 46 may be received from the programmable logic fabric 12 at a different rate than the

received data words 56 are provided to the programmable logic fabric 12.

[0028] As one of average skill in the art will appreciate, each of the modules within the PMA module 32 and PCS module 34 may be individually programmed to support a desired data transfer rate. The data transfer rate may be in accordance with a particular standard, such that the receive path, i.e., the programmable receive PMA module 40 and the programmable receive PCS module 44, may be programmed in accordance with one standard while the transmit path, i.e., the programmable transmit PCS module 42 and the programmable transmit PMA module 38, may be programmed in accordance with another standard.

[0029] Figure 3 illustrates a schematic block diagram of the programmable receive PMA module 40 that includes a programmable front-end 100, a data and clock recovery module 102, and a serial-to-parallel module 104. The programmable front-end 100, which will be described in greater detail with reference to Figures 4 - 8D, includes a tunable gain stage 108 and control module 106. The data and clock recovery module 102 includes a data detection circuit 110 and a phase locked loop 112. The phase locked loop 112 includes a phase detection module 114, a loop filter 116, a voltage controlled oscillator 118, a 1st divider module 120, and a 2nd divider module 122.

[0030] The programmable front-end 100 is operably coupled to receive the receive serial data 52 and produce amplified and equalized receive serial data 124 therefrom. To achieve this, the tunable gain stage 108 is programmed in accordance with an equalization setting 128 and an amplification setting 130, as produced by the control module 106, to provide the appropriate equalization and amplification of the received serial data 52.

[0031] The data and clock recovery circuit 102 receives the amplified and equalized receive serial data 124 via the phase detection module 114 of phase locked loop 112 and via

the data detection circuit 110. The phase detection module 114 has been initialized prior to receiving the amplified and equalized receive serial data 124 by comparing the phase and/or frequency of the reference clock 86 with a feedback reference clock produced by divider module 120. Based on this phase and/or frequency difference, the phase detection module 114 produces a corresponding current that is provided to loop filter 116. The loop filter 116 converts the current into a control voltage that adjusts the output frequency of the voltage controlled oscillator 118. The divider module 120, based on a serial received clock setting 132, divides the output oscillation produced by the VCO 118 to produce the feedback signal. Once the amplified and equalized receive serial data is received, the phase detection module 114 compares the phase of the amplified and equalized receive serial data 124 with the phase of the amplified and equalized receive serial data 124. Based on a phase difference between the amplified and equalized receive serial data 124 and the feedback signal, a current signal is produced.

[0032] The phase detection module 114 provides the current signal to the loop filter 116, which converts it into a control voltage that controls the output frequency of the voltage controlled oscillator 118. At this point, the output of the voltage controlled oscillator 118 corresponds to a recovered clock 138. The recovered clock 138 is provided to the divider module 122, the data detection circuit 110 and to the serial-to-parallel module 104. The data detection module 110 utilizes the recovered clock 138 to recovered data 136 from the amplified equalized receive serial data 124. The divider module 122 divides the recovered clock 138, in accordance with a parallel receive and programmable logic clock setting 134, to produce the parallel receive clock 94 and the programmable logic receive clock 96. Note that the serial receive clock setting 132 and the parallel receive and programmable logic clock setting 134 are part of the

programmable deserialization setting 66 provided to the programmable receive PMA module 40 by the control module 35.

[0033] The serial-to-parallel module 104, which may include an elastic store buffer, receives the recovered data 136 at a serial rate in accordance with the recovered clock 138. Based on a serial-to-parallel setting 135 and the parallel receive clock 194, the serial-to-parallel module 104 outputs the receive parallel data 54. The serial-to-parallel setting 135, which may be part of the programmable deserialization setting 66, indicates the rate and data width of the receive parallel data 54.

[0034] Figure 4 is a schematic block diagram of a programmable front-end 100 that includes control module 106 and a tunable gain stage 108. The tunable gain stage 108 includes a frequency dependent load 140 and an amplifier input section 142. The tunable gain stage 108 will be described in greater detail with reference to Figures 6 and 7.

[0035] The control module 106 generates an equalization setting 128 based on the channel response of the channel on which the receive serial data 52 is received. The control module 106 provides the equalization setting 128 to the frequency dependent load 140. The control module may also provide an amplification setting 130 to the tunable gain stage 108 based on the signal strength of the receive serial data 52.

[0036] The frequency dependent load 140, based on the equalization setting 128 and/or the amplification setting 130, adjusts its frequency response. The amplifier input section 142, in combination with the adjusted frequency dependent load 140, amplifies the received serial data 52 to produce amplified and equalized received serial data 124. In one embodiment, the frequency dependent load 140 includes at least one high-pass filter.

[0037] Figure 5 is an alternate schematic block diagram of a programmable front-end 100 that includes a tunable gain

stage 108 and control module 106. The tunable gain stage 108 includes 3 stages (stage 1, stage 2 and stage 3), which will be described in greater detail with reference to Figures 6 - 8D, that each receive the equalization setting 128 and/or amplification setting 130 from control module 106. As shown, stage 1 receives the received serial data 52, amplifies it, equalizes it, and passes its output to stage 2 which further amplifies and equalizes the signal which passes its output to stage 3 which further amplifies and equalizes the signal to produce the amplified and equalized received serial data 124. In this embodiment, stages 1 and 2 may be considered 1st and 2nd input stages while stage 3 may be considered an output stage of the tunable gain stage 108. As one of average skill in the art will appreciate, stages 1, 2 and 3 may be individually programmed via the control module 106 and/or programmed utilizing the same equalization setting.

[0038] Figure 6 is a schematic block diagram of an embodiment of the tunable gain stage 108 of Figure 4 and/or one of the stages of the tunable gain stage of Figure 5. In this embodiment, the frequency dependent load 140 includes a plurality of high-pass filters that are produced by the combination of NMOS transistors, resistors R1, R2, R3, R4 and capacitors C1, C2, C3 and C4. Note that capacitor having the designation C_p corresponds to the parasitic capacitance of the NMOS transistors. As one of average skill in the art will appreciate, resistors R1-R4 may be adjustable such that the frequency response of the corresponding high-pass filter may be tuned in accordance with the equalization setting. Further, the high-pass filter formed by R1, C_p, and C1 may be selectively enabled or disabled to further adjust the overall transfer characteristic of the frequency dependent load 140. Similarly, R4, C_p, and C4 may be enabled or disabled to adjust the overall transfer characteristic of the frequency dependent load 140. As one of average skill in the art will further appreciate, capacitors C1, C2, C3 and C4 may be omitted depending on the size of the parasitic capacitance C_p

and the desired corner frequency or frequencies of the high-pass filter or filters.

[0039] The amplifier input section 142 includes a pair of NMOS input transistors that receive the received serial data 52 and are coupled to a current source. As such, the frequency dependent load 140 acts as the load for amplifier input section 142. Since the frequency dependent load 140 includes the high-pass filtering established by resistors R1-R4, capacitors C1-C4, and parasitic capacitance, the amplification of the signal also includes a filtering, or equalization, of the signal, which results in the amplified and equalized received serial data 124.

[0040] Figure 6A is a schematic block diagram of another embodiment of the tunable gain stage 108 of Figure 4 and/or one of the stages of the tunable gain stage of Figure 5. In this embodiment, the frequency dependent load 140 includes a plurality of high-pass filters that are produced by the combination of NMOS transistors, resistors R5, R6, R7, R8 and capacitors C5 and C6. As shown, resistors R5 and R8 are variable resistors that are adjustable to tune the corresponding RC high pass filter (i.e., the high pass filter produced by the resistor, e.g., R5 (or R8) and the associated capacitor, e.g., C5 (or C6)) to obtain the desired corner frequency. Further, resistors R6 and R7 provide loading for the amplifier such that the output impedance, voltage levels, and/or power levels of the gain stage are at desired values. In yet another embodiment, C5 and C6 are the parasitic capacitances of their associated transistors.

[0041] The amplifier input section 142 includes a pair of NMOS input transistors that receive the received serial data 52 and are coupled to a current source. As such, the frequency dependent load 140 acts as the load for amplifier input section 142. Since the frequency dependent load 140 includes the high-pass filtering established by resistors R5 and R8 and the capacitors C5 and C6, the amplification of the signal also includes a filtering, or equalization, of the

signal, which results in the amplified and equalized received serial data 124.

[0042] Figure 7 is a schematic block diagram of a single-ended signaling tunable gain stage 108 or one of the stages of the tunable gain stage of Figure 5. In this embodiment, the frequency dependent load 140 includes resistors R1 and R2, capacitors C1 and C2, NMOS transistors and its corresponding parasitic capacitance (C_p). The amplifier input section 142 includes an input transistor and current source. In combination, the amplifier input section 142 and frequency dependent load amplifies and equalizes the received serial data 152 to produce the amplified and equalized received serial data 124.

[0043] As one of average skill in the art will appreciate, the frequency dependent load 140 shown in Figures 6 and/or 7 may include more or less resistor-capacitor combinations to further fine tune the high-pass filtering, or equalization, provided by the tunable gain stage. Further, the resistors and/or capacitors may be adjustable and individually enabled to adjust the high-pass filtering, and/or equalization, provided by the tunable gain stage 108.

[0044] Figure 8A is a schematic block diagram of a channel between two programmable logic devices 10. As shown, the channel includes a transmission line (TX line), a connector, a 2nd transmission line, a 2nd connector and a 3rd transmission line. This configuration is typical for integrated circuits mounted on different printed circuit boards where the printed circuit boards are coupled via a backplane. In this configuration, the integrated circuits may be up to a meter apart. At this distance, for high-speed serial data, the channel response will be significant and require appropriate equalization.

[0045] Figure 8B illustrates a channel that includes a single transmission line between programmable logic devices 10 that may be on the same printed circuit board. In this example, the length of the channel is much shorted than that

of Figure 8A. As such, its channel response will have less adverse affects on high-speed data than the channel of Figure 8A.

[0046] Figure 8C illustrates the channel response for the channels of Figures 8A and 8B. As shown, the channel for Figure 8A has a corner frequency that occurs at a frequency lower than the channel response for the channel of Figure 8B. In addition, the attenuation rate may be greater for the channel of Figure 8A than for Figure 8B. In addition, Figure 8C illustrates the data transmission rates that may traverse the channels of Figures 8A and 8B. As shown, a 3.125 gigabits-per-second transmission rate occurs at a lower frequency than 6.25 gigabits-per-second, which, in turn, is less than the 10 gigabits-per-second.

[0047] As is further shown for the 3.125 gigabits-per-second rate, the channel response for the channel of Figure 8B has minimal effect on the data being transmitted while the channel of Figure 8A begins to attenuate the data transmissions at the 3.125 gigabits-per-second rate. As is known, attenuation distorts the signals and thus reduces the receiver's sensitivity. As further shown, the 6.25 gigabits-per-second rate is significantly attenuated by the channel of Figure 8A and is somewhat attenuated by the channel of Figure 8B. The 10 gigabits-per-second rate is significantly attenuated by either channel.

[0048] Figure 8D illustrates the programmable equalization provided by the programmable analog front-end of the present invention. As shown, the equalization for 3.125 gigabits-per-second rate may be set to compensate for the channel response of Figures 8A or 8B. As the transmission rate increases and/or the channel response increases (i.e., the channel length increases), the amount of attenuation increases thus requiring the equalization to increase. As shown, the programmed equalization is significantly greater for 6.25 gigabits-per-second than it was for 3.125 gigabits-per-second and is even greater for 10 gigabits-per-second.

[0049] The preceding discussion has presented a programmable analog front-end that includes built-in equalization. By tuning the equalization within the analog front-end, the channel response for various channels may be more appropriately compensated thus improving the receiver sensitivity, which in turn increases the reliability of high speed data transmissions. As one of average skill in the art will appreciate, other embodiments may be derived from the teaching of the present invention without deviating from the scope of the claims.

CLAIMS

What is claimed is:

1. An analog front-end having built-in equalization, the analog front-end comprises:

control module operably coupled to provide a frequency response setting based on a channel response of a channel providing high-speed serial data to the analog front end; and

tunable gain stage operably coupled to amplify and equalize the high-speed serial data based on the frequency response setting, wherein the tunable gain stage includes:

a frequency dependent load that is adjusted based on the frequency response setting; and

amplifier input section operably coupled to the frequency dependent load, wherein the amplifier input section receives the high-speed serial data and, in conjunction with the frequency dependent load amplifies and equalizes the high-speed serial data to produce an amplified and equalized serial data.

2. The analog front-end of claim 1, wherein the tunable gain stage further comprises:

a first stage operably coupled to amplify and equalize, to a first level, the high-speed serial data based on the frequency response setting to produce a first amplified and equalized serial data; and

a second stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data.

3. The analog front-end of claim 2, wherein the second stage further comprises:

an input stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce intermediate amplified and equalized serial data; and

an output stage operably coupled to amplify and equalize the intermediate amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data.

4. The analog front-end of claim 1, wherein the frequency dependent load further comprises at least one high pass filter.

5. The analog front-end of claim 4, wherein each of the at least one high pass filter further comprises:

a transistor having a gate, a drain, and a source;

an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance value of the adjustable resistor is set based on the frequency response setting, and wherein parasitic capacitance of the transistor and the adjustable resistor establish a corner frequency for the each of the at least one high pass filter.

6. The analog front-end of claim 5, wherein the each of the at least one high pass filter further comprises:

a capacitor operably coupled between the gate and source of the transistor, wherein the capacitor, the parasitic capacitance and the adjustable resistor establish the corner frequency for the each of the at least one high pass filter.

7. The analog front-end of claim 1, wherein the tunable gain stage further comprises:

the frequency dependent load including:

a transistor having a gate, a drain, and a source;

an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance

value of the adjustable resistor is set based on the frequency response setting;

the amplifier input section including:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive, as a single-ended signal, the high-speed serial data, and the drain of the input transistor is operably coupled to the source of the transistor to provide the amplified and equalized serial data; and

current source operably coupled to the source of the input transistor and to a voltage return.

8. The analog front-end of claim 1, wherein the tunable gain stage further comprises:

the frequency dependent load including:

a first transistor having a gate, a drain, and a source;

a first adjustable resistor operably coupled to the gate and the drain of the first transistor, wherein a resistance value of the first adjustable resistor is set based on the frequency response setting;

a second transistor having a gate, a drain, and a source;

a second adjustable resistor operably coupled to the gate and the drain of the second transistor, wherein a resistance value of the second adjustable resistor is set based on the frequency response setting;

the amplifier input section including:

a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor is operably coupled to receive, as one leg of a differential signal, the high-speed serial data, and the drain of the first input transistor is operably

coupled to the source of the first transistor to provide one leg of the amplified and equalized serial data;

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive, as another leg of a differential signal, the high-speed serial data, and the drain of the second input transistor is operably coupled to the source of the second transistor to provide another leg of the amplified and equalized serial data;

current source operably coupled to the sources of the first and second input transistors and to a voltage return.

9. An analog front-end having built-in equalization, the analog front-end comprises:

a frequency dependent load; and

amplifier input section operably coupled to the frequency dependent load, wherein the amplifier input section receives high-speed serial data and, in conjunction with the frequency dependent load, amplifies and equalizes the high-speed serial data to produce an amplified and equalized serial data.

10. The analog front-end of claim 9, wherein the frequency dependent load further comprises at least one high pass filter.

11. The analog front-end of claim 10, wherein each of the at least one high pass filter further comprises:

a transistor having a gate, a drain, and a source;

a resistor operably coupled to the gate and the drain of the transistor, wherein parasitic capacitance of the transistor and the resistor establish a corner frequency for the each of the at least one high pass filter.

12. The analog front-end of claim 11, wherein the each of the at least one high pass filter further comprises:

a capacitor operably coupled between the gate and source of the transistor, wherein the capacitor, the parasitic capacitance and the resistor establish the corner frequency for the each of the at least one high pass filter.

13. The analog front-end of claim 9 further comprises:

the frequency dependent load including:

a transistor having a gate, a drain, and a source;

a resistor operably coupled to the gate and the drain of the transistor;

the amplifier input section including:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive, as a single-ended signal, the high-speed serial data, and the drain of the input transistor is operably coupled to the source of the transistor to provide the amplified and equalized serial data; and

current source operably coupled to the source of the input transistor and to a voltage return.

14. The analog front-end of claim 9 further comprises:

the frequency dependent load including:

a first transistor having a gate, a drain, and a source;

a first resistor operably coupled to the gate and the drain of the first transistor;

a second transistor having a gate, a drain, and a source;

a second resistor operably coupled to the gate and the drain of the second transistor;

the amplifier input section including:

a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor is operably coupled to receive, as one leg of a differential signal, the high-speed serial data, and the drain of the first input transistor is operably coupled to the source of the first transistor to provide one leg of the amplified and equalized serial data;

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive, as another leg of a differential signal, the high-speed serial data, and the drain of the second input transistor is operably coupled to the source of the second transistor to provide another leg of the amplified and equalized serial data;

current source operably coupled to the sources of the first and second input transistors and to a voltage return.

15. The analog front-end of claim 9 further comprises:
the frequency dependent load including:
a first frequency dependent load; and
a second frequency dependent load;
the amplifier input section including:

a first amplifier input section operably coupled to the first frequency dependent load, wherein the first amplifier input section receives the high-speed serial data and, in conjunction with the first frequency dependent load, amplifies and equalizes the high-speed serial data to produce an intermediate amplified and equalized serial data; and

a second amplifier input section operably coupled to the second frequency dependent load, wherein the second amplifier input section receives the intermediate amplified and equalized high-speed serial data and, in conjunction with the second frequency dependent load,

amplifies and equalizes the high-speed serial data to produce the amplified and equalized serial data.

16. A high-speed data receiver comprises:

an analog front-end operably coupled to amplify and equalize high-speed data to produce amplified and equalized high-speed data; and

clock and data recovery module operably coupled to recover a clock signal and data from the amplified and equalized high-speed data, wherein the analog front-end includes:

control module operably coupled to provide a frequency response setting based on a channel response of a channel providing the high-speed data to the analog front end; and

tunable gain stage operably coupled to amplify and equalize the high-speed data based on the frequency response setting, wherein the tunable gain stage includes:

a frequency dependent load that is adjusted based on the frequency response setting; and

amplifier input section operably coupled to the frequency dependent load, wherein the amplifier input section receives the high-speed data and, in conjunction with the frequency dependent load amplifies and equalizes the high-speed data to produce an amplified and equalized serial data.

17. The high-speed data receiver of claim 16, wherein the tunable gain stage further comprises:

a first stage operably coupled to amplify and equalize, to a first level, the high-speed data based on the frequency response setting to produce a first amplified and equalized serial data; and

a second stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data.

18. The high-speed data receiver of claim 17, wherein the second stage further comprises:

an input stage operably coupled to amplify and equalize the first amplified and equalized serial data based on the frequency response setting to produce intermediate amplified and equalized serial data; and

an output stage operably coupled to amplify and equalize the intermediate amplified and equalized serial data based on the frequency response setting to produce the amplified and equalized serial data.

19. The high-speed data receiver of claim 16, wherein the frequency dependent load further comprises at least one high pass filter.

20. The high-speed data receiver of claim 19, wherein each of the at least one high pass filter further comprises:

a transistor having a gate, a drain, and a source;

an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance value of the adjustable resistor is set based on the frequency response setting, and wherein parasitic capacitance of the transistor and the adjustable resistor establish a corner frequency for the each of the at least one high pass filter.

21. The high-speed data receiver of claim 20, wherein the each of the at least one high pass filter further comprises:

a capacitor operably coupled between the gate and source of the transistor, wherein the capacitor, the parasitic capacitance and the adjustable resistor establish the corner frequency for the each of the at least one high pass filter.

22. The high-speed data receiver of claim 16, wherein the tunable gain stage further comprises:
the frequency dependent load including:
a transistor having a gate, a drain, and a source;
an adjustable resistor operably coupled to the gate and the drain of the transistor, wherein a resistance value of the adjustable resistor is set based on the frequency response setting;
the amplifier input section including:
an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive, as a single-ended signal, the high-speed data, and the drain of the input transistor is operably coupled to the source of the transistor to provide the amplified and equalized serial data; and
current source operably coupled to the source of the input transistor and to a voltage return.

23. The high-speed data receiver of claim 16, wherein the tunable gain stage further comprises:
the frequency dependent load including:
a first transistor having a gate, a drain, and a source;
a first adjustable resistor operably coupled to the gate and the drain of the first transistor, wherein a resistance value of the first adjustable resistor is set based on the frequency response setting;
a second transistor having a gate, a drain, and a source;
a second adjustable resistor operably coupled to the gate and the drain of the second transistor, wherein a resistance value of the second adjustable resistor is set based on the frequency response setting;

the amplifier input section including:

a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor is operably coupled to receive, as one leg of a differential signal, the high-speed data, and the drain of the first input transistor is operably coupled to the source of the first transistor to provide one leg of the amplified and equalized serial data;

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive, as another leg of a differential signal, the high-speed data, and the drain of the second input transistor is operably coupled to the source of the second transistor to provide another leg of the amplified and equalized serial data;

current source operably coupled to the sources of the first and second input transistors and to a voltage return.

24. A high-speed data receiver comprises:

an analog front-end operably coupled to amplify and equalize high-speed data to produce amplified and equalized high-speed data; and

clock and data recovery module operably coupled to recover a clock signal and data from the amplified and equalized high-speed data, wherein the analog front-end includes:

a frequency dependent load; and

amplifier input section operably coupled to the frequency dependent load, wherein the amplifier input section receives high-speed data and, in conjunction with the frequency dependent load, amplifies and equalizes the high-speed data to produce an amplified and equalized serial data.

25. The high-speed data receiver of claim 24, wherein the frequency dependent load further comprises at least one high pass filter.

26. The high-speed data receiver of claim 25, wherein each of the at least one high pass filter further comprises:

a transistor having a gate, a drain, and a source;

a resistor operably coupled to the gate and the drain of the transistor, wherein parasitic capacitance of the transistor and the resistor establish a corner frequency for the each of the at least one high pass filter.

27. The high-speed data receiver of claim 26, wherein the each of the at least one high pass filter further comprises:

a capacitor operably coupled between the gate and source of the transistor, wherein the capacitor, the parasitic capacitance and the resistor establish the corner frequency for the each of the at least one high pass filter.

28. The high-speed data receiver of claim 24, wherein the analog front-end further comprises:

the frequency dependent load including:

a transistor having a gate, a drain, and a source;

a resistor operably coupled to the gate and the drain of the transistor;

the amplifier input section including:

an input transistor having a gate, a drain, and a source, wherein the gate of the input transistor is operably coupled to receive, as a single-ended signal, the high-speed data, and the drain of the input transistor is operably coupled to the source of the transistor to provide the amplified and equalized serial data; and

current source operably coupled to the source of the input transistor and to a voltage return.

29. The high-speed data receiver of claim 24, wherein the analog front-end further comprises:
the frequency dependent load including:

a first transistor having a gate, a drain, and a source;

a first resistor operably coupled to the gate and the drain of the first transistor;

a second transistor having a gate, a drain, and a source;

a second resistor operably coupled to the gate and the drain of the second transistor;

the amplifier input section including:

a first input transistor having a gate, a drain, and a source, wherein the gate of the first input transistor is operably coupled to receive, as one leg of a differential signal, the high-speed data, and the drain of the first input transistor is operably coupled to the source of the first transistor to provide one leg of the amplified and equalized serial data;

a second input transistor having a gate, a drain, and a source, wherein the gate of the second input transistor is operably coupled to receive, as another leg of a differential signal, the high-speed data, and the drain of the second input transistor is operably coupled to the source of the second transistor to provide another leg of the amplified and equalized serial data;

current source operably coupled to the sources of the first and second input transistors and to a voltage return.

30. The high-speed data receiver of claim 24, wherein the analog front-end further comprises:

the frequency dependent load including:

a first frequency dependent load; and

a second frequency dependent load;

the amplifier input section including:

a first amplifier input section operably coupled to the first frequency dependent load, wherein the first amplifier input section receives the high-speed data and, in conjunction with the first frequency dependent load, amplifies and equalizes the high-speed data to produce an intermediate amplified and equalized serial data; and

a second amplifier input section operably coupled to the second frequency dependent load, wherein the second amplifier input section receives the intermediate amplified and equalized high-speed data and, in conjunction with the second frequency dependent load, amplifies and equalizes the high-speed data to produce the amplified and equalized serial data.

ANALOG FRONT-END HAVING BUILT-IN EQUALIZATION AND APPLICATIONS THEREOF

ABSTRACT OF THE DISCLOSURE

An analog front-end having built-in equalization includes a control module and a tunable gain stage. The control module is operably coupled to provide a frequency response setting based on a channel response of a channel providing high-speed serial data to the analog front-end. The tunable gain stage includes a frequency dependent load and an amplifier input section. The frequency dependent load is adjusted based on the frequency response setting. The amplifier input section is operably coupled to the frequency dependent load and receives the high-speed serial data. In conjunction with the frequency dependent load, the amplifier input section amplifies and equalizes the high-speed serial data to produce an amplified and equalized serial data.

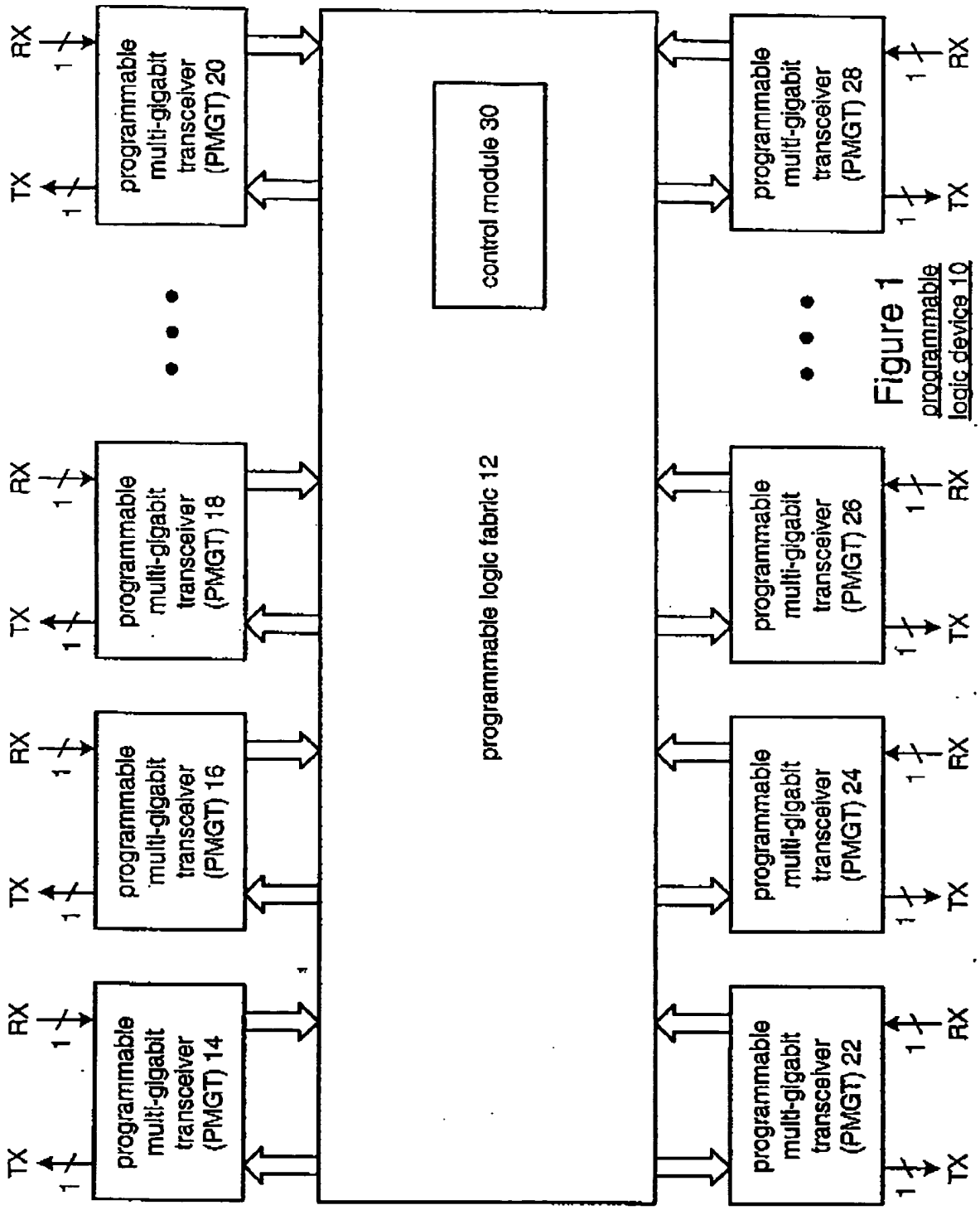

Figure 1 programmable logic device 10

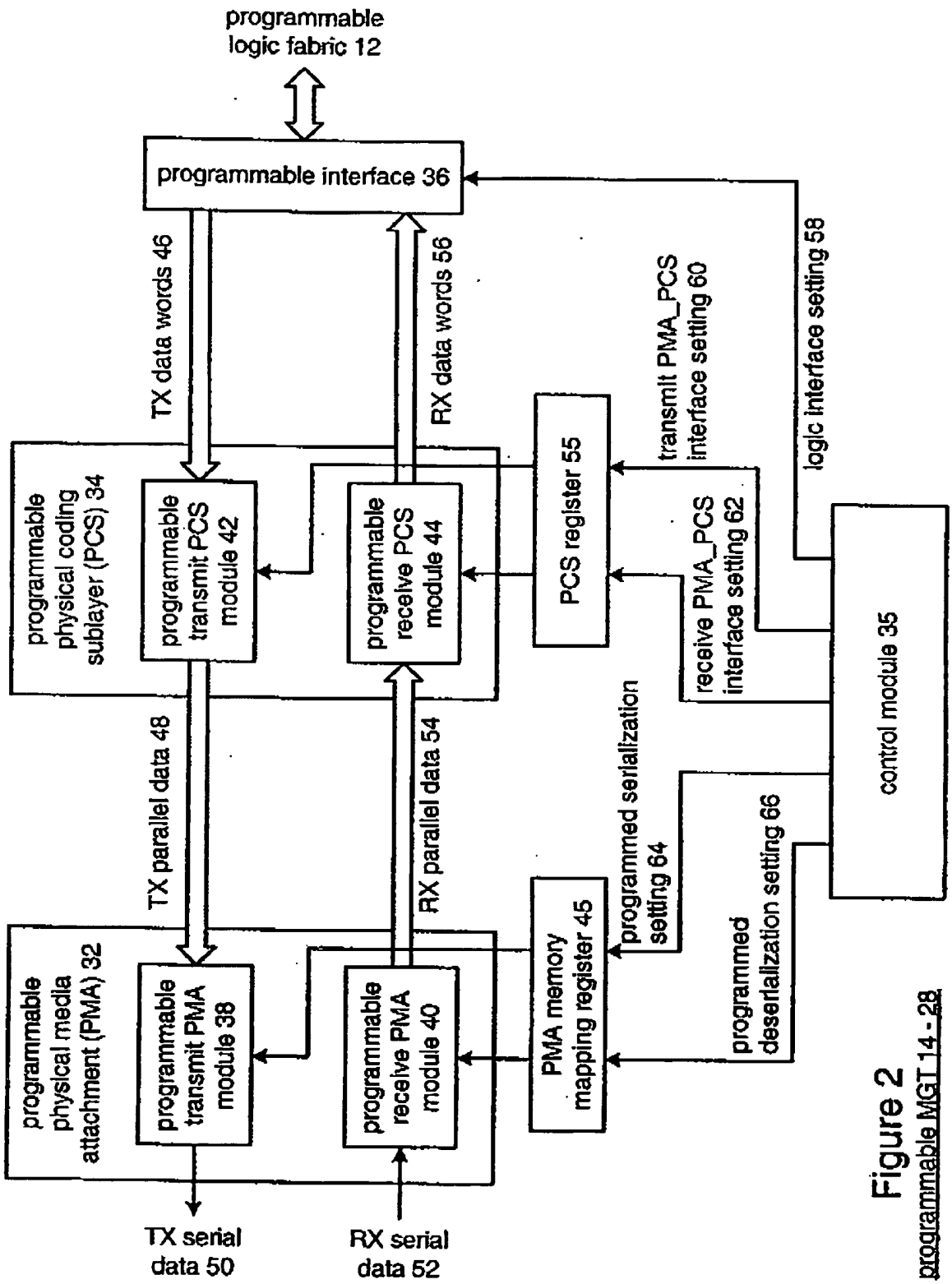

Figure 2
programmable MGT 14 - 28

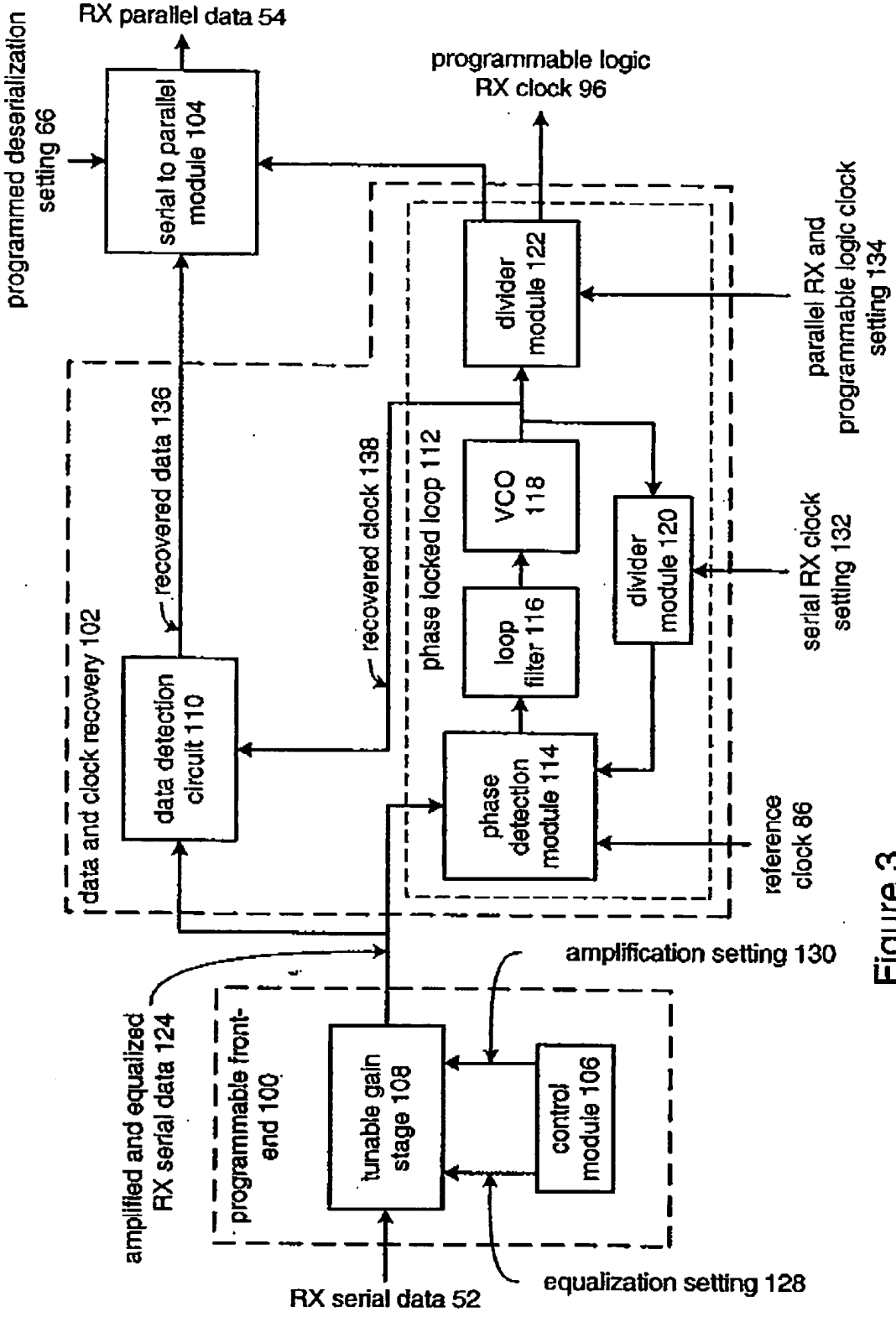

Figure 3
programmable receive PMA module 40

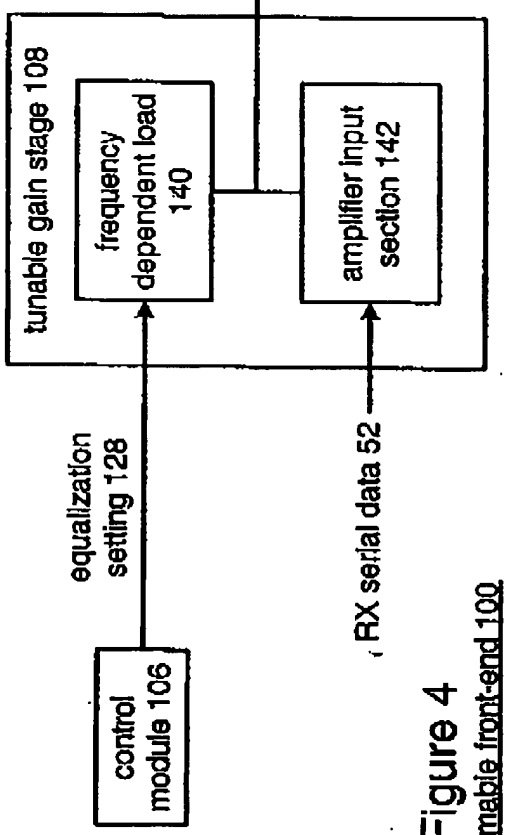

Figure 4
programmable front-end 100

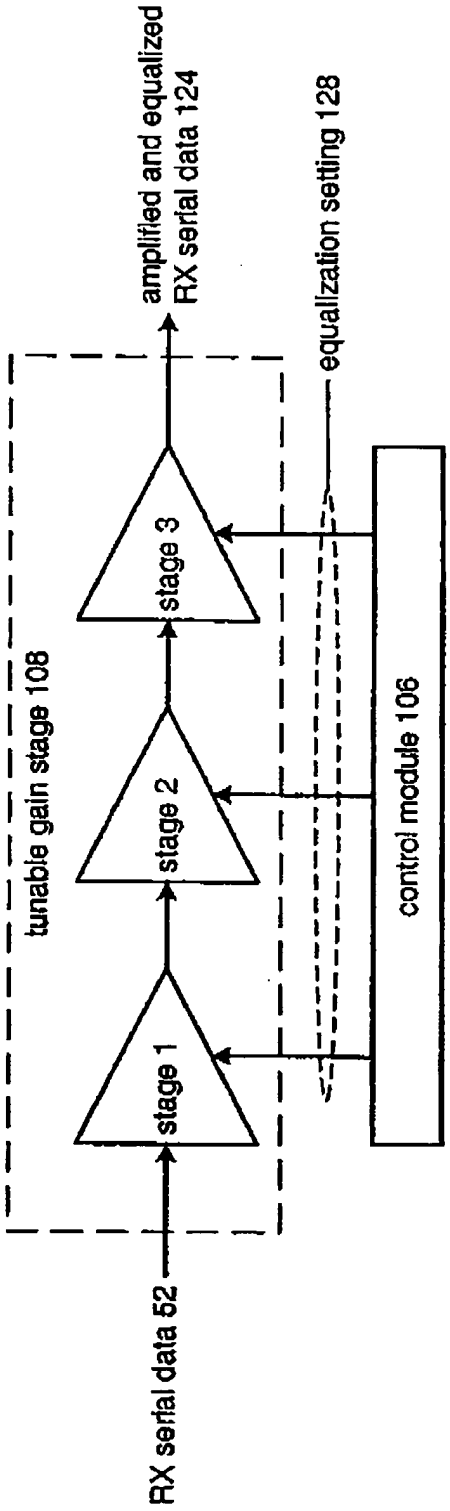

Figure 5
programmable front-end 100

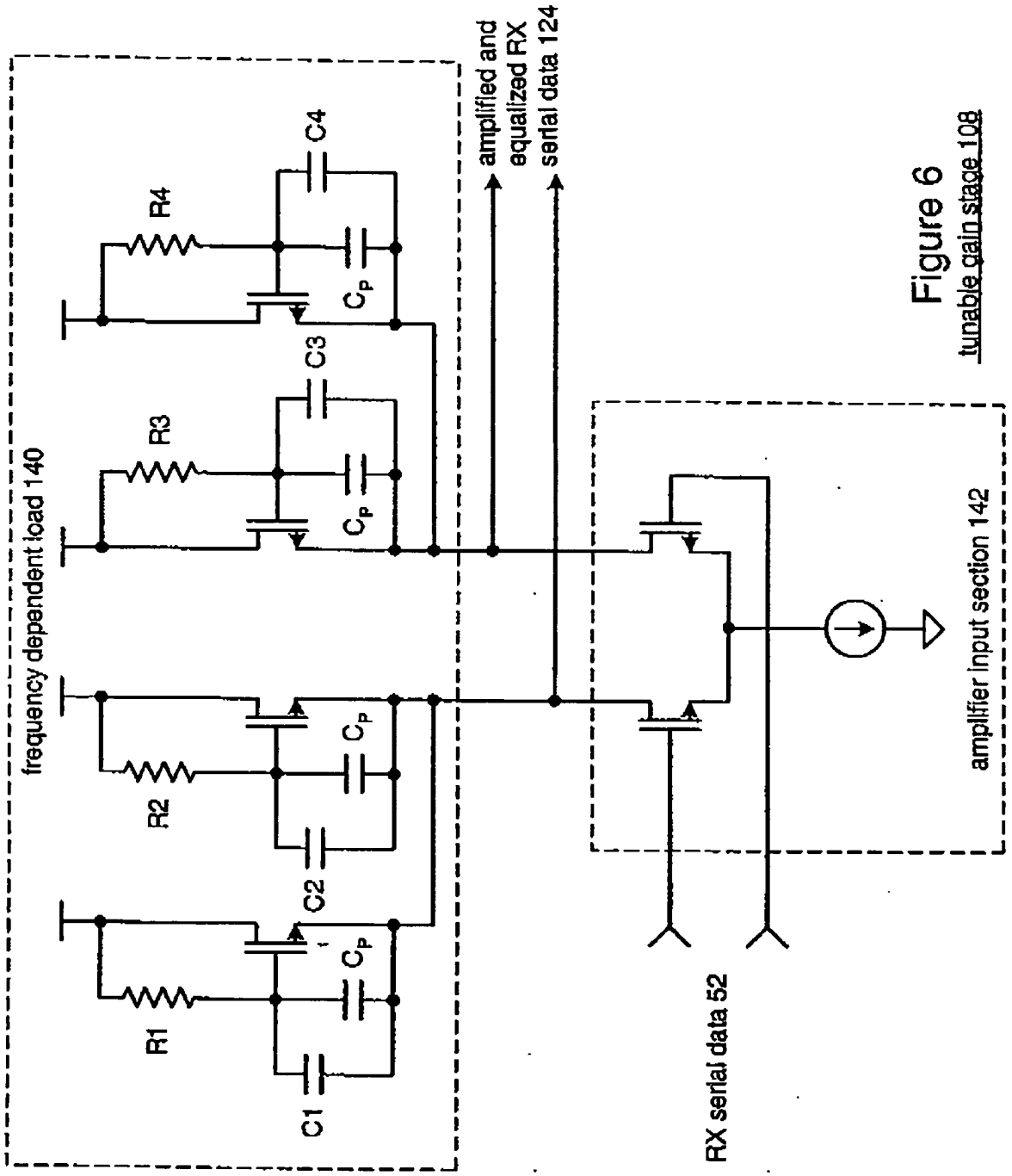

Figure 6
tunable gain stage 108

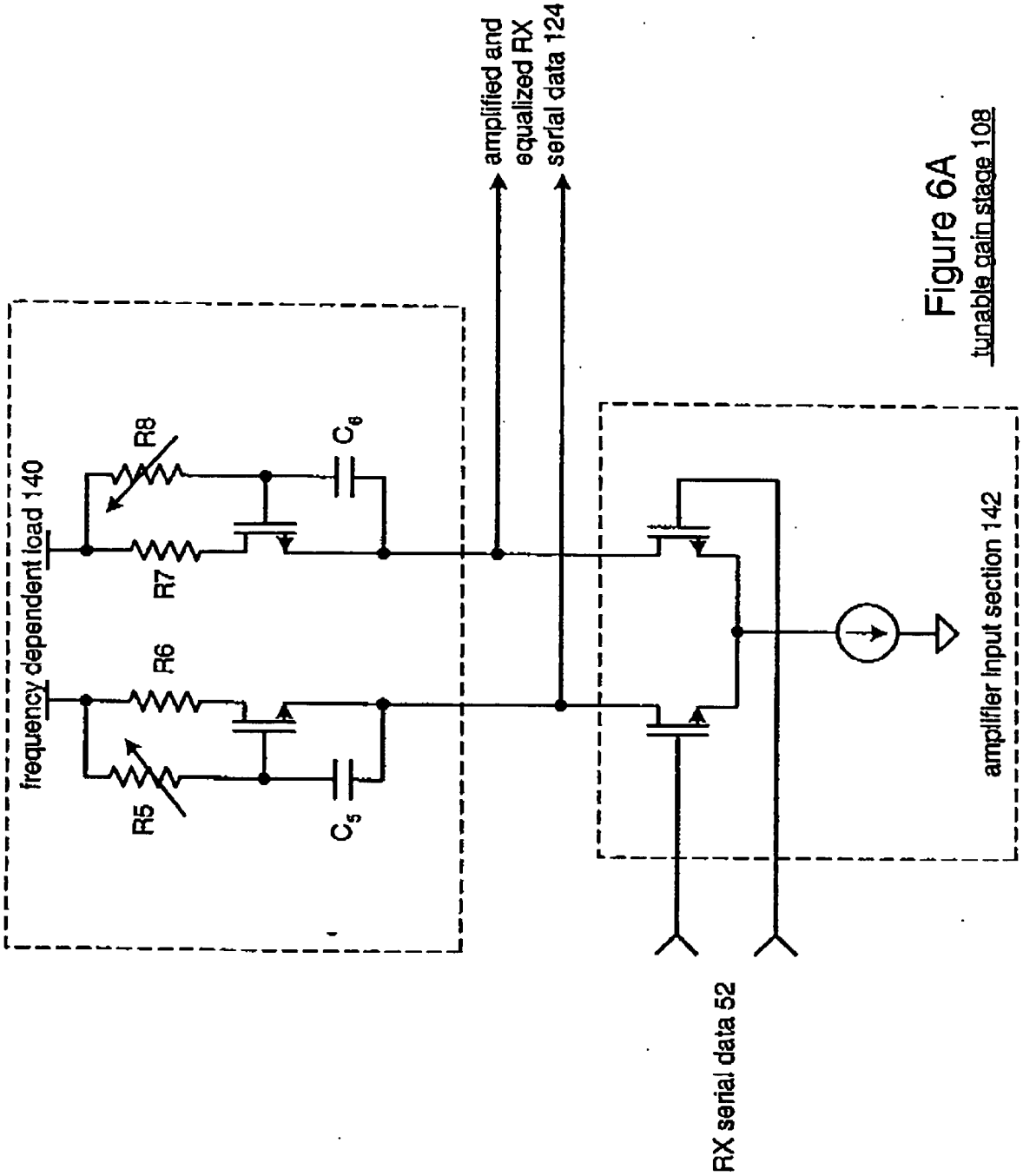

Figure 6A
tunable gain stage 108

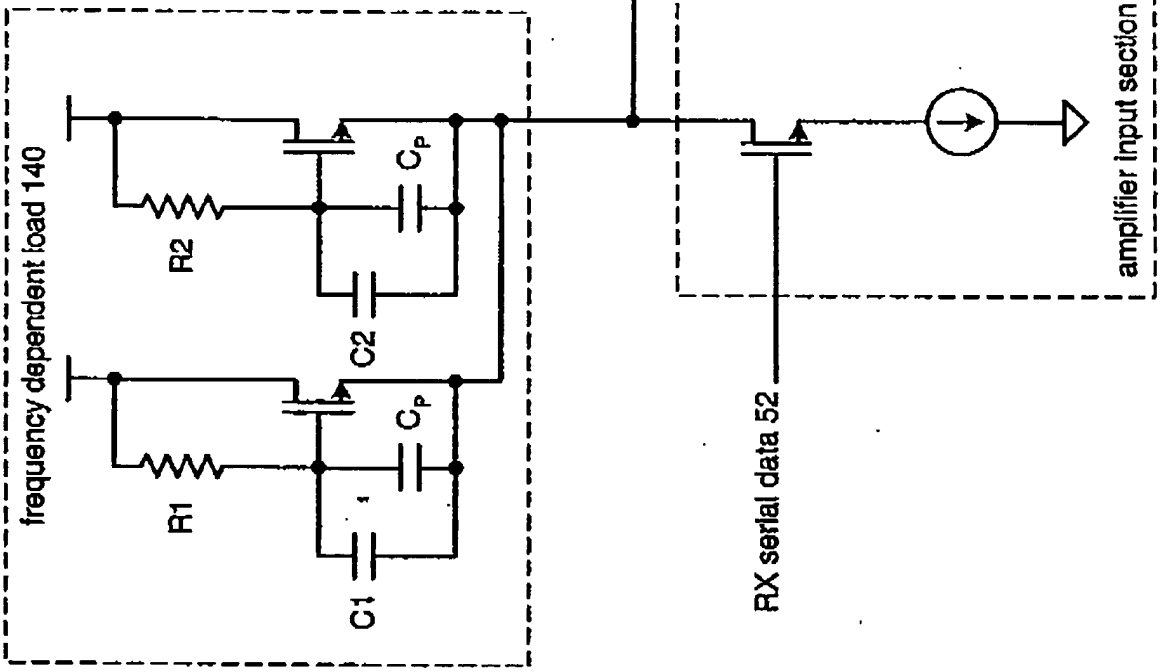

Figure 7
tunable gain stage 108

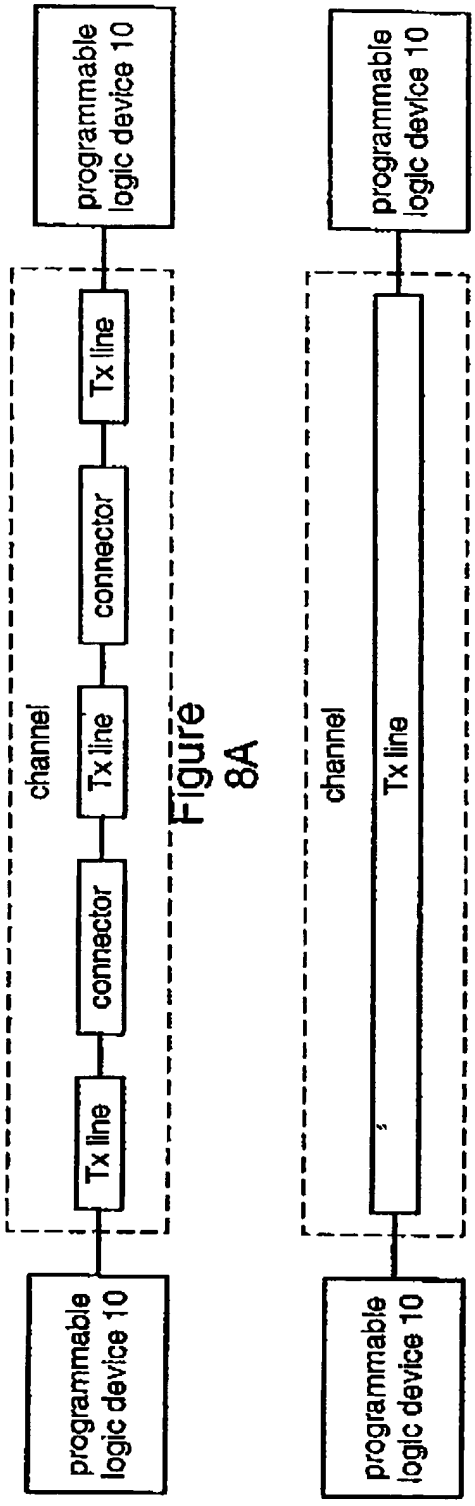

Figure 8A

Figure 8B

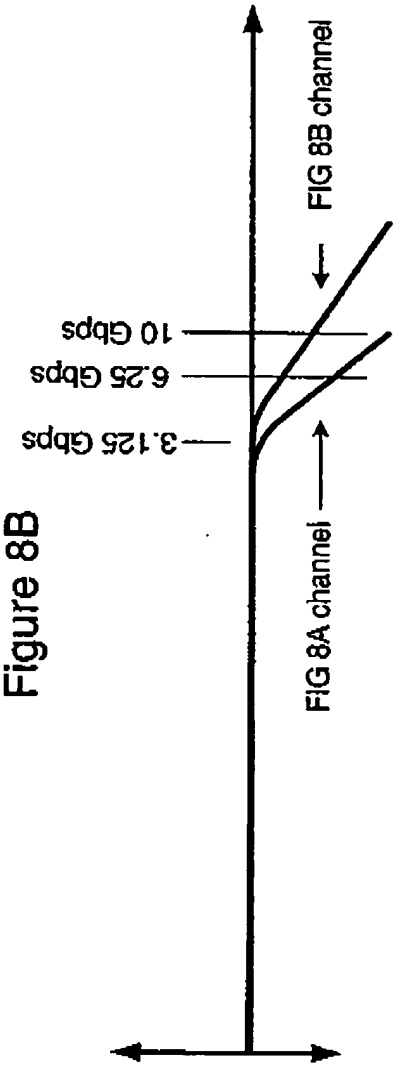

Figure 8C
channel response

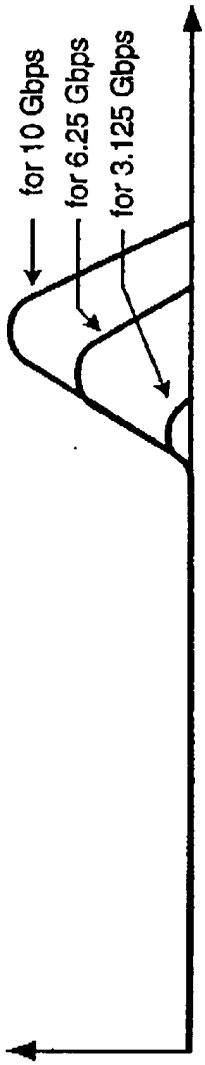

Figure 8D
programmable equalization

X-1358 US PATENT

10/659,971
09-11-03

RECEIVER TERMINATION NETWORK AND APPLICATION THEREOF

Charles W. Boecker
William C. Black
Eric D. Groen

FIELD OF THE INVENTION

[0001] This invention relates generally to communication systems and more particularly to an enhanced data conveyance within such communication systems.

BACKGROUND OF THE INVENTION

[0002] Communication systems are known to transport large amounts of data between a plurality of end user devices. Such end user devices include telephones, facsimile machines, computers, television sets, cellular phones, personal digital assistants, et cetera. As is also known, such communication systems may be a local area network (LAN) and/or a wide area network (WAN). A local area network is generally understood to be a network that interconnects a plurality of end user devices distributed over a localized area (e.g., up to a radius of 10 kilometers) and includes LAN infrastructure equipment. For example, a local area network may be used to interconnect workstations distributed within an office of a single building or a group of buildings, to interconnect computer based equipment distributed around a factory or hospital, et cetera. As is further known, local area networks may be wired local area networks or wireless local area networks. Wired local area networks typically have a star topology, ring topology, bus topology or hub/tree topology.

[0003] A wide area network is generally understood to be a network that covers a wide geographic area and includes WAN infrastructure equipment. Wide area networks include both public data networks and enterprise wide private data networks. A public data network is established and operated by a national network administrator specifically for data

transmission. Such public data networks facilitate the inner working of equipment from different manufacturers. Accordingly, standards by the ITU-T have been established for conveying data within public data networks. Currently, there are two main types of public data networks: packet switched public data networks and circuit switched public data networks. For example, the public switched telephone network is a circuit switched public data network while the Internet is a packet switched public data network. Other examples of wide area networks include integrated service digital networks (ISDN) and broadband multiservice networks.

[0004] As is further known, communication systems may be networked together to yield larger communication systems, where such networking is typically referred to as internetworking. Internetworking is achieved via internetworking units that allow communication networks using the same or different protocols to be linked together. The internetworking units may be routers, gateways, protocol converters, bridges, and/or switches.

[0005] Regardless of the type of communication system (e.g., LAN, WAN, or internetworking system), each communication system employs a data conveyance protocol to ensure that data is accurately conveyed within the system. In general, a protocol is a formal set of rules and conventions that govern how system devices (e.g., end user devices, LAN infrastructure equipment, WAN infrastructure equipment, and/or internetworking units) exchange data within the communication system. Such protocols typically include regulations on receiver sensitivity (i.e., how noisy a received signal may be and how small its amplitude may be) for signals received by a system device or within a system device, and on transmit power of a signal from one system device to another or within the system device.

[0006] As is further known, each system device may process millions of bits of data per second or more. Accordingly, each system device includes high-speed data interfaces to input and output data efficiently. Such

interfaces are typically implemented as integrated circuits that are mounted on a printed circuit board. A group of printed circuit boards may be mounted on a backplane and multiple backplanes may further be placed in a rack to make up the system device.

[0007] In an effort to meet the ever-increasing challenges of improving data conveyance speed, each system device includes an increasing number of integrated circuits, printed circuit boards (PCBs), and/or racks. Typically, the racks and PCBs are coupled together using coaxial cables, fiber optics, connectors, and/or wires. The integrated circuits on a printed circuit board are operably coupled together via copper traces (e.g., FR4 connections). As the number and complexity of the system devices increase, the distance between ICs, PCBs, and/or racks is increasing and is more diverse. For instance, some communication channels between ICs, PCBs, and/or racks may have one type of termination requirement (e.g., 50 Ohm DC coupling to V_{DD}, V_{SS}, or a mid-supply voltage), while others have a different type of termination requirement (e.g., 50 Ohm AC coupling).

[0008] To accommodate for the various types of channel termination, the termination had to be done off chip, i.e., the components that provide the termination are on the PCB. This requires additional components on the PCB and makes using an integrated circuit more complicated. It further increases the cost of the PCB.

[0009] Therefore, a need exists for programmable receiver termination network for use within receiver sections of high-speed data interfaces.

BRIEF SUMMARY OF THE INVENTION

[0010] The receiver termination network in accordance with the present invention substantially meets these needs and others. In one embodiment, the receiver termination network is included in a high-speed receiver that also includes a receiver analog front-end and a data recovery

module. The receiver termination network includes a DC matched termination circuit and an AC coupled bias circuit. The DC matched termination circuit is operably coupled to provide a termination of a transmission line coupling the high-speed receiver to a transmission source and to receive high-speed data via the transmission line. The AC coupled bias circuit is operably coupled to provide a common mode reference and to high-pass filter the high-speed data to produce filtered high-speed data. The receiver analog front-end is biased in accordance with the common mode reference and is operably coupled to amplify the filtered high-speed data to produce amplified high-speed data. The data recovery module is operably coupled to recover data from the amplified high-speed data. The receiver termination network may be programmed for use within a variety of high-speed receivers that have varying termination requirements.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 is a schematic block diagram of a programmable logic device in accordance with the present invention;

[0012] Figure 2 is a schematic block diagram of a programmable multi-gigabit transceiver in accordance with the present invention;

[0013] Figure 3 is a schematic block diagram of a programmable receive physical media attachment (PMA) module in accordance with the present invention;

[0014] Figure 4 is a schematic block diagram of a receiver termination network in accordance with the present invention;

[0015] Figure 5 is an alternate schematic block diagram of a receiver termination network in accordance with the present invention;

[0016] Figure 6 is a schematic block diagram of a further alternate embodiment of a receiver termination network in accordance with the present invention;

[0017] Figure 7 is a graphical representation of an integrated circuit implementation of the capacitors used within the receiver termination network in accordance with the present invention; and

[0018] Figure 8 is a schematic block diagram of an equivalent circuit of the capacitor of Figure 7.

DETAILED DESCRIPTION OF THE INVENTION

[0019] Figure 1 is a schematic block diagram of a programmable logic device 10 that includes programmable logic fabric 12, a plurality of programmable multi-gigabit transceivers (PMGT) 14-28 and a control module 30. The programmable logic device 10 may be, for instance, a programmable logic array device, a programmable array logic device, an erasable programmable logic device, and/or a field programmable gate array (FPGA). When the programmable logic device 10 is a field programmable gate array (FPGA), the programmable logic fabric 12 may be implemented as a symmetric array configuration, a row-based configuration, a sea-of-gates configuration, and/or a hierarchical programmable logic device configuration. The programmable logic fabric 12 may further include at least one dedicated fixed processor, such as a microprocessor core, to further facilitate the programmable flexibility offered by a programmable logic device 10.

[0020] The control module 30 may be contained within the programmable logic fabric 12 or it may be a separate module. In either implementation, the control module 30 generates the control signals to program each of the transmit and receive sections of the programmable multi-gigabit transceivers 14-28. In general, each of the programmable multi-gigabit transceivers 14-28 performs a serial-to-parallel conversion on received data and performs a

parallel-to-serial conversion on transmit data. The parallel data may be 8-bits, 16-bits, 32-bits, 64-bits, et cetera wide. Typically, the serial data will be a 1-bit stream of data that may be a binary level signal, multi-level signal, etc. Further, two or more programmable multi-gigabit transceivers may be bonded together to provide greater transmitting speeds. For example, if multi-gigabit transceivers 14, 16 and 18 are transceiving data at 3.125 gigabits-per-second, the transceivers 14-18 may be bonded together such that the effective serial rate is 3 times 3.125 gigabits-per-second.

[0021] Each of the programmable multi-gigabit transceivers 14-28 may be individually programmed to conform to separate standards. In addition, the transmit path and receive path of each multi-gigabit transceiver 14-28 may be separately programmed such that the transmit path of a transceiver is supporting one standard while the receive path of the same transceiver is supporting a different standard. Further, the serial rates of the transmit path and receive path may be programmed from 1 gigabit-per-second to tens of gigabits-per-second. The size of the parallel data in the transmit and receive sections, or paths, is also programmable and may vary from 8-bits, 16-bits, 32-bits, 64-bits, et cetera.

[0022] Figure 2 is a schematic block diagram of one embodiment of a representative one of the programmable multi-gigabit transceivers 14-28. As shown, the programmable multi-gigabit transceiver includes a programmable physical media attachment (PMA) module 32, a programmable physical coding sub-layer (PCS) module 34, a programmable interface 36, a control module 35, a PMA memory mapping register 45 and a PCS register 55. The control module 35, based on the desired mode of operation for the individual programmable multi-gigabit transceiver 14-28, generates a programmed deserialization setting 66, a programmed serialization setting 64, a receive PMA_PCS interface setting 62, a transmit PMA_PCS interface setting

60, and a logic interface setting 58. The control module 35 may be a separate device within each of the multi-gigabit transceivers and/or included within the control module 30. In either embodiment of the PMGT control module 35, the programmable logic device control module 30 determines the corresponding overall desired operating conditions for the programmable logic device 10 and provides the corresponding operating parameters for a given multi-gigabit transceiver to its control module 35, which generates the settings 58-66.

[0023] The programmable physical media attachment (PMA) module 32 includes a programmable transmit PMA module 38 and a programmable receive PMA module 40. The programmable transmit PMA module 38 is operably coupled to convert transmit parallel data 48 into transmit serial data 50 in accordance with the programmed serialization setting 64. The programmed serialization setting 64 indicates the desired rate of the transmit serial data 50, the desired rate of the transmit parallel data 48, and the data width of the transmit parallel data 48. The programmable receive PMA module 40, which will be described in greater detail with reference to Figure 3, is operably coupled to convert receive serial data 52 into receive parallel data 54 based on the programmed deserialization setting 66. The programmed deserialization setting 66 indicates the rate of the receive serial data 52, the desired rate of the receive parallel data 54, and the data width of the receive parallel data 54. The PMA memory mapping register 45 may store the serialization setting 64 and the deserialization setting 66.

[0024] The programmable physical coding sub-layer (PCS) module 34 includes a programmable transmit PCS module 42 and a programmable receive PCS module 44. The programmable transmit PCS module 42 receives transmit data words 46 from the programmable logic fabric 12 via the programmable interface 36 and converts them into the transmit parallel data 48 in accordance with the transmit PMA_PCS interface setting 60. The transmit PMA_PCS interface setting 60

indicates the rate of the transmit data words 46, the size of the transmit data words (e.g., 1-byte, 2-bytes, 3-bytes, 4-bytes, et cetera) and the corresponding transmission rate of the transmit parallel data 48. The programmable receive PCS module 44 converts the receive parallel data 54 into receive data words 56 in accordance with the receive PMA_PCS interface setting 62. The receive PMA_PCS interface setting 62 indicates the rate at which the receive parallel data 54 will be received, the width of the parallel data 54, the transmit rate of the receive data words 56 and the word size of the receive data words 56.

[0025] The control module 35 also generates the logic interface setting 58 that provides the rates at which the transmit data words 46 and receive data words 56 will be transceived with the programmable logic fabric 12. Note that the transmit data words 46 may be received from the programmable logic fabric 12 at a different rate than the receive data words 56 are provided to the programmable logic fabric 12.

[0026] As one of average skill in the art will appreciate, each of the modules within the PMA module 32 and PCS module 34 may be individually programmed to support a desired data transfer rate. The data transfer rate may be in accordance with a particular standard, such that the receive path, i.e., the programmable receive PMA module 40 and the programmable receive PCS module 44, may be programmed in accordance with one standard while the transmit path, i.e., the programmable transmit PCS module 42 and the programmable transmit PMA module 38, may be programmed in accordance with another standard.

[0027] Figure 3 illustrates a schematic block diagram of the programmable receive PMA module 40 that includes a programmable front-end 100, a data and clock recovery module 102, and a serial-to-parallel module 104. The programmable front-end 100 includes a receiver termination circuit 106 and a receiver amplifier 108. The data and clock recovery module 102 includes a data detection circuit 110 and a phase

locked loop 112. The phase locked loop 112 includes a phase detection module 114, a loop filter 116, a voltage controlled oscillator 118, a 1st divider module 120, and a 2nd divider module 122.

[0028] The programmable front-end 100, which will be described in greater detail with reference to Figures 4 - 8, is operably coupled to receive the receive serial data 52 and produce amplified and equalized receive serial data 124 therefrom. To achieve this, the receiver termination circuit 106 is programmed in accordance with a receive termination setting 126 to provide the appropriate termination for the transmission line between the programmable receiver PMA module 40 and the source that originally transmitted the receive serial data 52. The receive termination setting 126 may indicate, for instance, whether the receive serial data 52 is a single-ended signal or a differential signal, the impedance of the termination line, and the biasing of the receiver termination circuit 106.

[0029] The receiver termination circuit 106 further biases the receive serial data 52 and provides the bias adjusted signal to the receiver amplifier 108. The gain and equalization settings of the receiver amplifier 108 may be adjusted in accordance with the equalization setting 128 and the amplification setting 130, respectively. Note that the receive termination setting 126, the equalization setting 128, and the amplification setting 130 are part of the programmed deserialization setting 66 provided by the control module 35.

[0030] The data and clock recovery circuit 102 receives the amplified and equalized receive serial data 124 via the phase detection module 114 of phase locked loop 112 and via the data detection circuit 110. The phase detection module 114 has been initialized prior to receiving the amplified and equalized receive serial data 124 by comparing the phase and/or frequency of the reference clock 86 with a feedback reference clock produced by divider module 120. Based on

this phase and/or frequency difference, the phase detection module 114 produces a corresponding current that is provided to loop filter 116. The loop filter 116 converts the current into a control voltage that adjusts the output frequency of the voltage controlled oscillator 118. The divider module 120, based on a serial receive clock setting 132, divides the output oscillation produced by the VCO 118 to produce the feedback signal. Once the amplified and equalized receive serial data 124 is received, the phase detection module 114 compares the phase of the amplified and equalized receive serial data 124 with the phase of the feedback signal. Based on a phase difference between the amplified and equalized receive serial data 124 and the feedback signal, a current signal is produced.

[0031] The phase detection module 114 provides the current signal to the loop filter 116, which converts it into a control voltage that controls the output frequency of the voltage controlled oscillator 118. At this point, the output of the voltage controlled oscillator 118 corresponds to a recovered clock 138. The recovered clock 138 is provided to the divider module 122, the data detection circuit 110 and to the serial-to-parallel module 104 via the divider module 122. The data detection module 110 utilizes the recovered clock 138 to recover recovered data 136 from the amplified equalized receive serial data 124. The divider module 122 divides the recovered clock 138, in accordance with a parallel receive and programmable logic clock setting 134, to produce the parallel receive clock 94 and the programmable logic receive clock 96. Note that the serial receive clock setting 132 and the parallel receive and programmable logic clock setting 134 are part of the programmable deserialization setting 66 provided to the programmable receive PMA module 40 by the control module 35.

[0032] The serial-to-parallel module 104, which may include an elastic store buffer, receives the recovered data 136 at a serial rate in accordance with the recovered clock 138. Based on a serial-to-parallel setting 135 and the

parallel receive clock 94, the serial-to-parallel module 104 outputs the receive parallel data 54. The programmable deserialization setting 66 indicates the rate and data width of the receive parallel data 54.

[0033] Figure 4 is a schematic block diagram of the receiver termination circuit, or network, 106 that includes a DC matched termination circuit 140 and an AC coupled bias circuit 142. The DC matched termination circuit 140 receives the receive serial data 52 via a transmission line (TL). The DC termination circuit 140 provides a impedance matching the transmission line and is DC coupled to the transmission line. The DC matched termination circuit 140 will be described in greater detail with reference to Figures 5 and 6.

[0034] The AC coupled bias circuit 142 receives the receive serial data 52 via the DC matched termination circuit 140 and produces a common mode reference 144 therefrom and further filters the receive serial data 52 to produce filtered high-speed data 146. The common mode reference 144 is provided to the receiver amplifier 108 of the programmable front-end 100. The details of the AC coupled bias circuit 142 will be described in greater detail with reference to Figures 5 and 6.

[0035] Figure 5 illustrates a differential signaling implementation of the receiver termination circuit, or network, 106 that includes the DC matched termination circuit 140 and the AC coupled bias circuit 142. The DC matched termination circuit includes a pair of resistors R1 and R2 and an integrated circuit pad coupled to receive a receiver termination setting 126. The receiver termination setting 126 allows the DC matched termination circuit to be terminated with respect to V_{DD} (i.e., the supply voltage), V_{SS} (i.e., the supply return), or a mid-supply voltage. The values of resistors R1 and R2 are dependent on the impedance of the transmission line and the desired matched termination. For example, resistors R1 and R2 may be 50 Ohm resistors.

[0036] The AC coupled bias circuit 142 includes capacitors C1 and C2 and impedances R3 and R4, which may be resistors or unity gain transconductance amplifiers. Note that the impedance values of impedances R3 and R4 are significantly bigger than the impedance values of R1 and R2. For example, impedances R3 and R4 may be 1 mega Ohm resistors or unity gain transconductance amplifiers having a transconductance value that corresponds to the inverse of the resistance values (e.g., 1/(1 mega Ohm)). Capacitors C1 and C2 provide AC coupling of the receive serial data 52 to the receiver amplifier 108. In addition, C1, C2, R3 and R4 provide a high-pass filter, with a corner frequency established by the values of the resistors and capacitors, for the receive serial data 52, thereby producing the filtered high-speed data 146. As is further shown, the tap of impedances R3 and R4 are coupled to a bias voltage (V_{bias}). The bias voltage may be set to a particular level to provide the common mode reference 144 for the receiver amplifier 108. As such, the receiver termination network 106 is programmable via the receiver termination setting 126 and/or via the bias voltage V_{bias}. Note that if the unity gain transconductance amplifiers are used for impedances R3 and R4, then their non-inverting inputs coupled together and to the bias voltage and their inverting inputs are coupled to the input lines, respectively.

[0037] Figure 6 illustrates a single-ended implementation of the receiver termination circuit, or network, 106. In this embodiment, the DC matched termination circuit 140 includes resistor R1, which is coupled across the transmission line. The resistance value of R1 is selected to match the impedance of the transmission line and/or the desired termination impedance. The AC coupled bias circuit 142 includes capacitor C1 and resistor R2. Capacitor C1 AC couples the receive serial data 52 to the receiver amplifier 108. In addition, capacitor C1 in combination with resistor R2 provide a high-pass filter for the receive serial data 52 such that the signal provided to the receiver amplifier 108

is filtered. The bias level of the receiver amplifier may be adjusted via the bias voltage (V_{bias}). Note that resistor R2 may optionally be connected to V_{bias} (as shown by the dashed line) or another voltage.

[0038] The capacitors C1 and C2 of Figure 5 and the capacitor C1 of Figure 6 may be fabricated on an integrated circuit in accordance with the integrated circuit diagram of Figure 7. As shown, the capacitor includes a 1st plate 150, a 2nd plate 152, and a doping block 154. The 1st plate is fabricated on the same metal layer as the 2nd plate 152 and both have an interlacing finger design. As one of average skill in the art will appreciate, the 1st plate 150 and 2nd plate 152 may be fabricated on multiple metal layers connected with vias to provide greater surface area. The doping block 154 encompasses the 1st and 2nd plates to provide resistance in series with the parasitic capacitance produced by the 1st and 2nd plates 150 and 152. The doping block 154 may comprise a doping material that provides a resistance with respect to ground.

[0039] Figure 8 is a schematic block diagram illustrating an equivalent circuit of the capacitor of Figure 7. Capacitor C1, as indicated in Figure 8, is produced via the 1st and 2nd plates 150 and 152 of Figure 7. The plates 150 and 152 produce parasitic capacitors 160 with respect to ground and/or to the substrate. The doping block adds resistance 162 in series with the parasitic capacitor 160. In one embodiment, the doping block resistance 162 is about 2 kilo Ohms, which, in series with the parasitic capacitance 160, substantially reduces the adverse effects of the parasitic capacitance 160. Note that the capacitance value of C1 and C2 may be approximately 10 pico Farads.

[0040] The preceding discussion has presented a programmable receiver termination network that is programmable to facilitate a variety of termination requirements. By including a DC circuit and AC coupling circuit within the programmable network, high-pass filtering is achieved as well as providing the desired DC termination

and common mode biasing. As one of average skill in the art will appreciate, other embodiments may be derived from the teaching of the present invention without deviating from the scope of the claims.

CLAIMS

What is claimed is:

1. A high-speed receiver comprising:

a receiver termination network that includes:

a DC matched termination circuit operably coupled to provide a termination of a transmission line coupling the high-speed receiver to a transmission source and to receive high-speed data via the transmission line; and

an AC coupled bias circuit operably coupled to provide a common mode reference and to high pass filter the high-speed data to produce the filtered high-speed data;

a receiver analog front-end biased in accordance with the common mode reference, wherein the receiver analog front-end is operably coupled to amplify the filtered high-speed data to produce amplified high-speed data; and

a data recovery module operably coupled to recover data from the amplified high-speed data.

2. The high-speed receiver of claim 1, wherein the DC matched termination circuit comprises:

first resistor having an impedance corresponding to impedance of the transmission line; and

second resistor having an impedance corresponding to the impedance of the transmission line, wherein the first and second resistors are coupled in series and the series combination of the first and second resistors is coupled to the transmission line.

3. The high-speed receiver of claim 2, wherein the DC matched termination circuit further comprises:

a termination biasing integrated circuit pad operably coupled to a center node of the series combination of the first and second resistors to provide selective coupling of the center node to a supply voltage, to a supply return voltage, or to a mid-supply voltage for proper termination of the transmission source.

4. The high-speed receiver of claim 2, wherein the AC coupled bias circuit comprises:

first capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the first resistor;

second capacitor having a first plate and a second plate, wherein the first plate of the second capacitor is operably coupled to the second resistor;

first impedance having a first node operably coupled to the second plate of the first capacitor; and

second impedance having a first node operably coupled to the second plate of the second capacitor, wherein a second node of the first impedance is operably coupled to a second node of the second impedance and coupled to a bias voltage, wherein impedance of the first and second impedances is at least one order of magnitude greater than the impedance of the first and second resistors, and wherein capacitance of the first and second capacitors, in combination with the first and second impedances, establish a corner frequency for the high-pass filter.

5. The high-speed receiver of claim 4, wherein each of the first and second capacitors further comprises:

the first plate and second plate configured in a finger arrangement to produce a capacitor structure; and

a doping block encompassing the capacitor structure to provide an impedance in series with parasitic capacitance of the capacitor structure.

6. The high-speed receiver of claim 4, wherein each of the first and second capacitors further comprises:

the first plate being fabricated on at least two metal layers operably coupled with a first via; and

the second plate being fabricated on the at least two metal layers operably coupled with a second via.

7. The high-speed receiver of claim 1, wherein the DC matched termination circuit comprises:

a resistor having an impedance corresponding to impedance of the transmission line.

8. The high-speed receiver of claim 7, wherein the AC coupled bias circuit comprises:

a capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the resistor; and

a bias impedance having a first node operably coupled to the second plate of the first capacitor and a second node coupled to a supply return, wherein impedance of the bias impedance is at least one order of magnitude greater than the impedance of the resistor, and wherein capacitance of the capacitor, in combination with the bias impedance, establish a corner frequency for the high-pass filter.

9. A multi-gigabit transceiver comprising:

transmit section operably coupled to convert parallel output data into high-speed output serial data; and

receiver section that includes:

a receiver termination network that includes:

a DC matched termination circuit operably coupled to provide a termination of a transmission line coupling the high-speed receiver to a transmission source and to receive high-speed serial data via the transmission line; and

an AC coupled bias circuit operably coupled to provide a common mode reference and to high pass filter the high-speed serial data to produce the filtered high-speed serial data;

a receiver analog front-end biased in accordance with the common mode reference, wherein the receiver analog front-end is operably coupled to amplify the filtered high-speed serial data to produce amplified high-speed serial data; and

a data recovery module operably coupled to recover data from the amplified high-speed serial data.

10. The multi-gigabit transceiver of claim 9, wherein the DC matched termination circuit comprises:

first resistor having an impedance corresponding to impedance of the transmission line; and

second resistor having an impedance corresponding to the impedance of the transmission line, wherein the first and second resistors are coupled in series and the series combination of the first and second resistors is coupled to the transmission line.

11. The multi-gigabit transceiver of claim 10, wherein the DC matched termination circuit further comprises:

a termination biasing integrated circuit pad operably coupled to a center node of the series combination of the first and second resistors to provide selective coupling of the center node to a supply voltage, to a supply return voltage, or to a mid-supply voltage for proper termination of the transmission source.

12. The multi-gigabit transceiver of claim 10, wherein the AC coupled bias circuit comprises:

first capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the first resistor;

second capacitor having a first plate and a second plate, wherein the first plate of the second capacitor is operably coupled to the second resistor;

first impedance having a first node operably coupled to the second plate of the first capacitor; and

second impedance having a first node operably coupled to the second plate of the second capacitor, wherein a second node of the first impedance is operably coupled to a second node of the second impedance and coupled to a bias voltage, wherein impedance of the first and second impedances is at least one order of magnitude greater than the impedance of the first and second resistors, and wherein capacitance of the first and second capacitors, in combination with the first and second impedances, establish a corner frequency for the high-pass filter.

13. The multi-gigabit transceiver of claim 9, wherein the DC matched termination circuit comprises:

a resistor having an impedance corresponding to impedance of the transmission line.

14. The multi-gigabit transceiver of claim 13, wherein the AC coupled bias circuit comprises:

a capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the resistor; and

bias impedance having a first node operably coupled to the second plate of the first capacitor and a second node coupled to a supply return, wherein impedance of the bias impedance is at least one order of magnitude greater than the impedance of the resistor, and wherein capacitance of the capacitor, in combination with the bias impedance, establish a corner frequency for the high-pass filter.

15. An integrated circuit capacitor comprising:

a first plate fabricated on a metal layer having a first geometric shape;

a second plate fabricated on the metal layer having a second geometric shape, wherein the first and second geometric shapes form a finger arrangement to produce a capacitor structure; and

doping block encompassing the capacitor structure to provide an impedance in series with parasitic capacitance of the capacitor structure.

16. The integrated circuit capacitor of claim 15 further comprising:

the first plate further being fabricated on a second metal layer having the first geometric shape, wherein the first geometric shape of the second metal layer is coupled to the first geometric shape on the metal layer by a via; and

the second plate further being fabricated on the second metal layer having the second geometric shape, wherein the second geometric shape of the second metal layer is coupled to the second geometric shape on the metal layer by a second via.

17. A receiver termination network comprising:

a DC matched termination circuit operably coupled to provide a termination of a transmission line coupling a high-speed receiver to a transmission source and to receive high-speed data via the transmission line; and

an AC coupled bias circuit operably coupled to high pass filter the high-speed data to produce filtered high-speed data and operably coupled to produce a common mode reference.

18. The receiver termination network of claim 17, wherein the DC matched termination circuit comprises:

first resistor having an impedance corresponding to impedance of the transmission line; and

second resistor having an impedance corresponding to the impedance of the transmission line, wherein the first and second resistors are coupled in series and the series combination of the first and second resistors is coupled to the transmission line.

19. The receiver termination network of claim 18, wherein the DC matched termination circuit further comprises:

a termination biasing integrated circuit pad operably coupled to a center node of the series combination of the first and second resistors to provide selective coupling of the center node to a supply voltage, to a supply return voltage, or to a mid-supply voltage for proper termination of the transmission source.

20. The receiver termination network of claim 18, wherein the AC coupled bias circuit comprises:

first capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the first resistor;

second capacitor having a first plate and a second plate, wherein the first plate of the second capacitor is operably coupled to the second resistor;

first impedance having a first node operably coupled to the second plate of the first capacitor; and

second impedance having a first node operably coupled to the second plate of the second capacitor, wherein a second node of the first impedance is operably coupled to a second node of the second impedance and coupled to a bias voltage, wherein impedance of the first and second impedances is at least one order of magnitude greater than the impedance of the first and second resistors, and wherein capacitance of the first and second capacitors, in combination with the first and second impedances, establish a corner frequency for the high-pass filter.

21. The receiver termination network of claim 20, wherein each of the first and second capacitors further comprises:

the first plate and second plate configured in a finger arrangement to produce a capacitor structure; and

a doping block encompassing the capacitor structure to provide an impedance in series with parasitic capacitance of the capacitor structure.

22. The receiver termination network of claim 20, wherein each of the first and second capacitors further comprises:

the first plate being fabricated on at least two metal layers operably coupled with a first via; and

the second plate being fabricated on the at least two metal layers operably coupled with a second via.

23. The receiver termination network of claim 18, wherein the DC matched termination circuit comprises:

a resistor having an impedance corresponding to impedance of the transmission line.

24. The receiver termination network of claim 23, wherein the AC coupled bias circuit comprises:

a capacitor having a first plate and a second plate, wherein the first plate of the first capacitor is operably coupled to the resistor; and

a bias impedance having a first node operably coupled to the second plate of the first capacitor and a second node coupled to a supply return, wherein impedance of the bias impedance is at least one order of magnitude greater than the impedance of the resistor, and wherein capacitance of the capacitor, in combination with the bias impedance, establish a corner frequency for the high-pass filter.

ABSTRACT

A receiver termination network is included in a high-speed receiver that also includes a receiver analog front-end and a data recovery module. The receiver termination network includes a DC matched termination circuit and an AC coupled bias circuit. The DC matched termination circuit is operably coupled to provide a termination of a transmission line coupling the high-speed receiver to a transmission source and to receive high-speed data via the transmission line. The AC coupled bias circuit is operably coupled to provide a common mode reference and to high-pass filter the high-speed data to produce filtered high-speed data. The receiver analog front-end is biased in accordance with the common mode reference and is operably coupled to amplify the filtered high-speed data to produce amplified high-speed data.

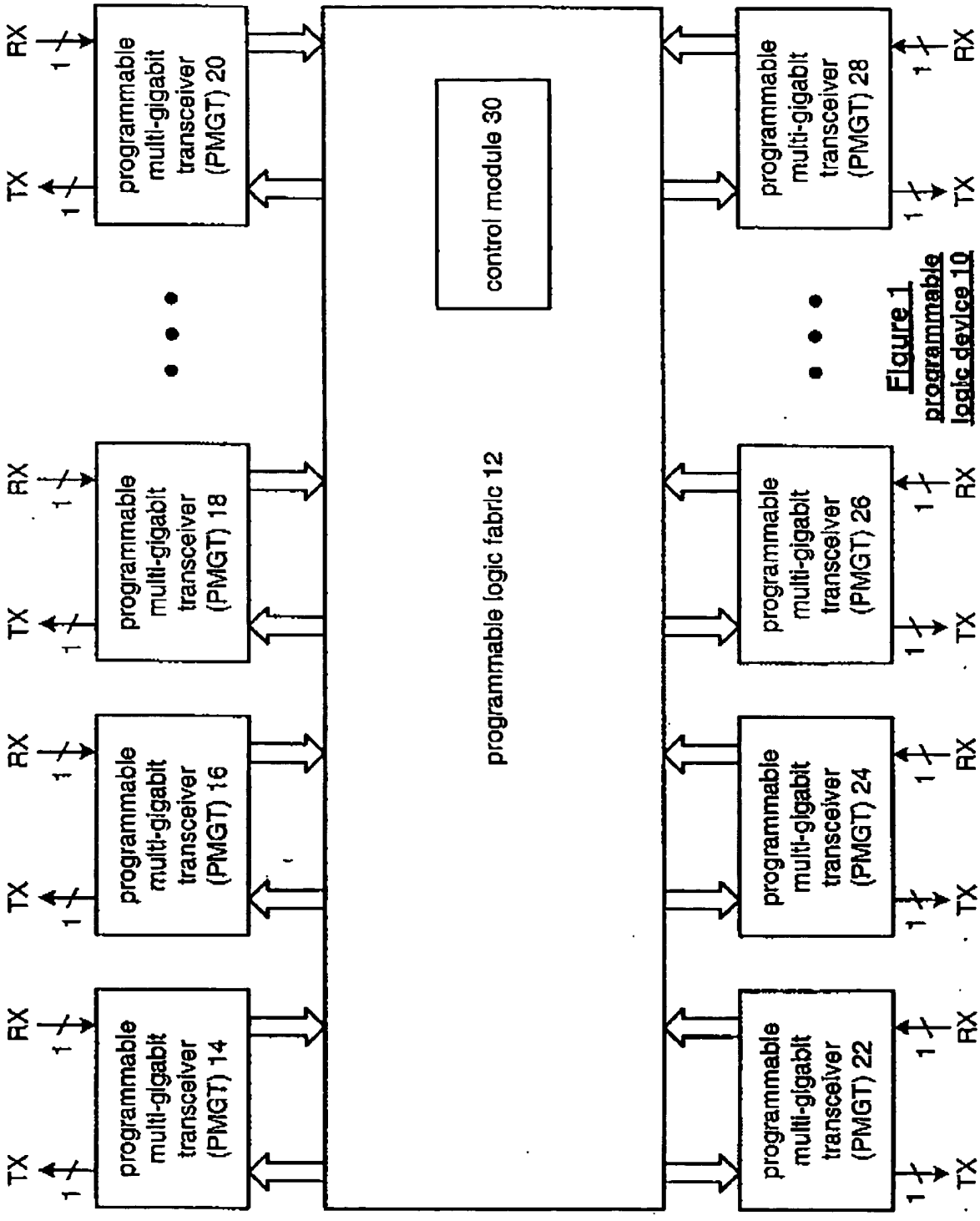

Figure 1 programmable logic device 10

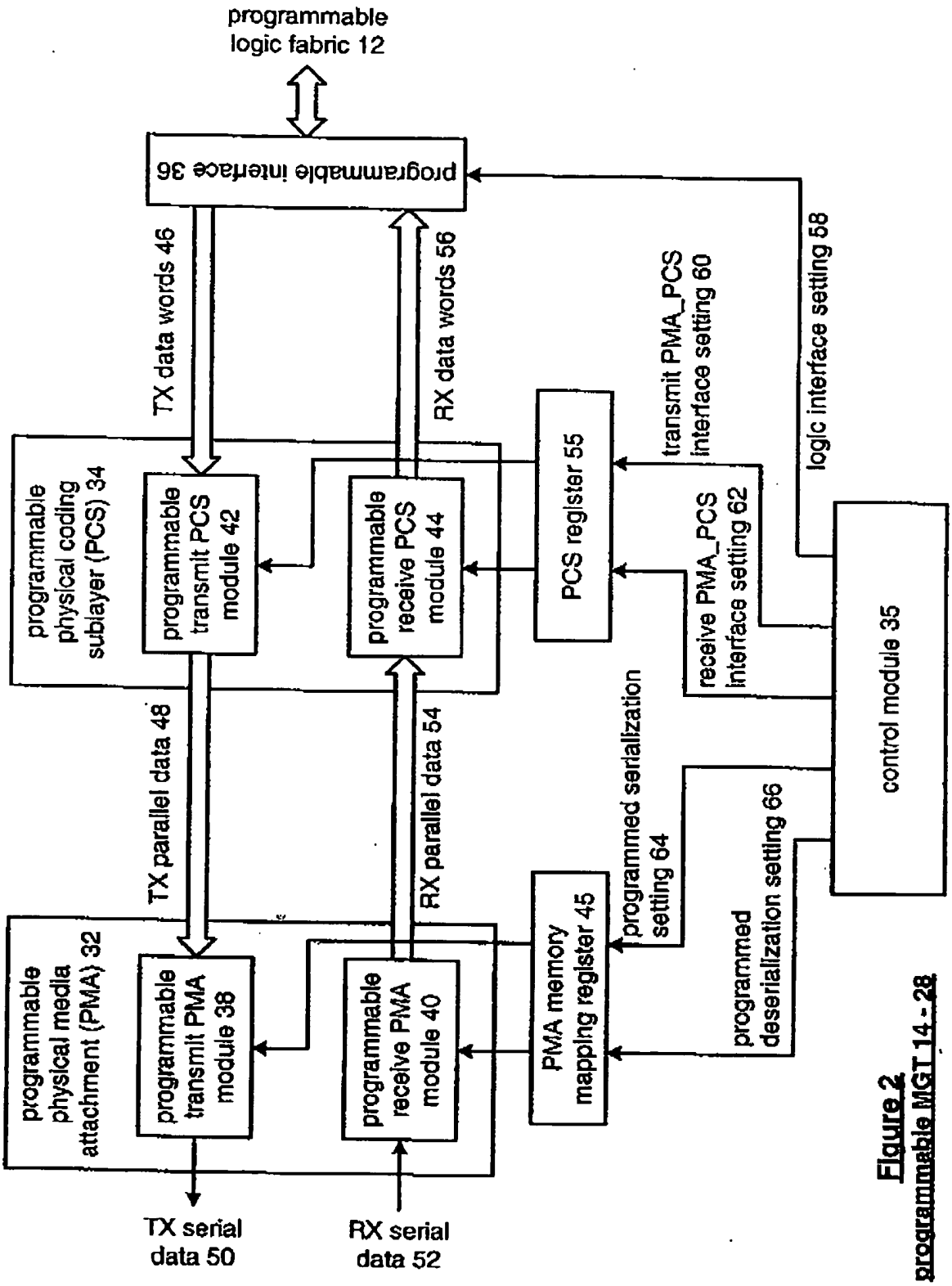

Figure 2
programmable MGT 14 - 28

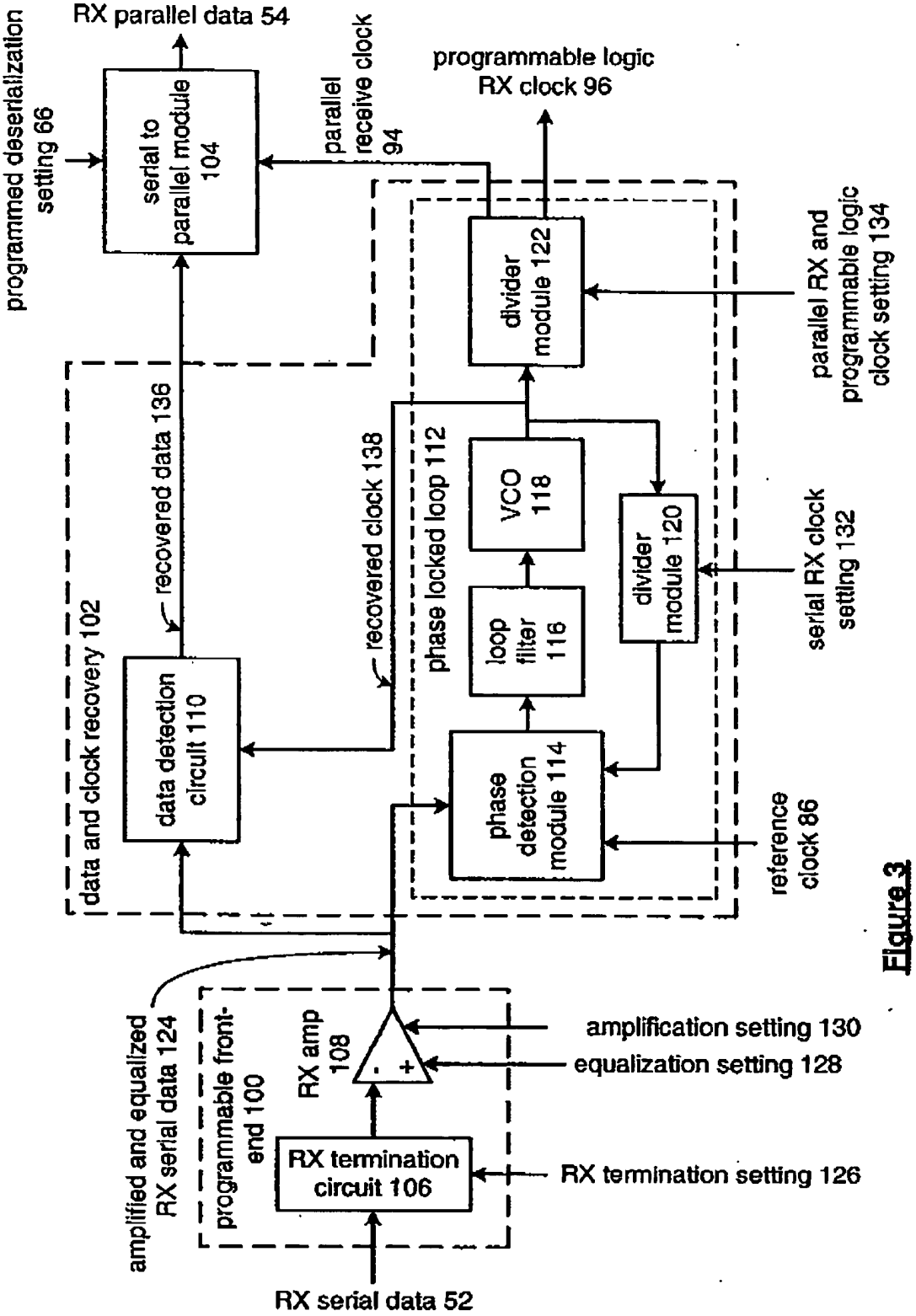

Figure 3
programmable receive PMA module 40

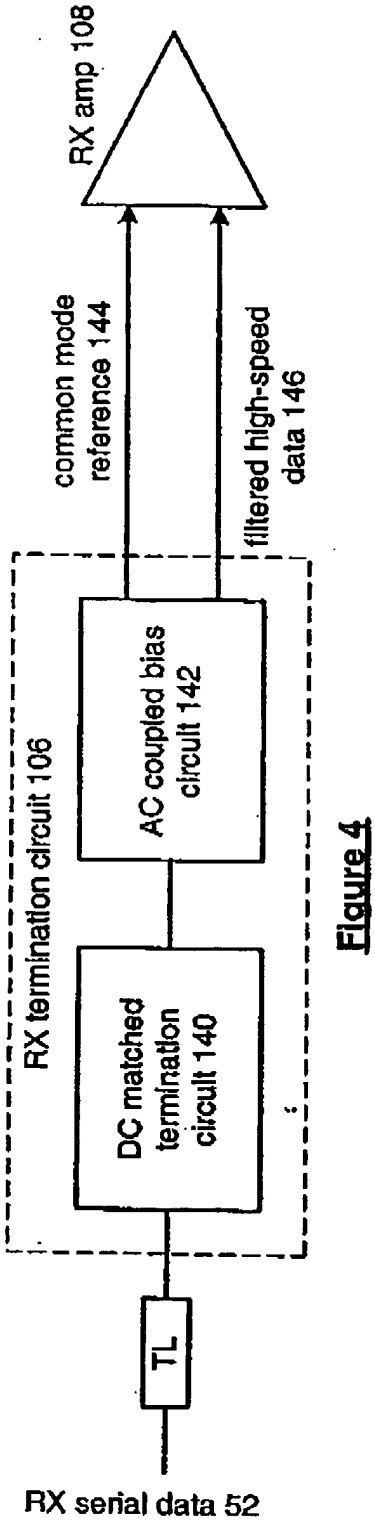

Figure 4

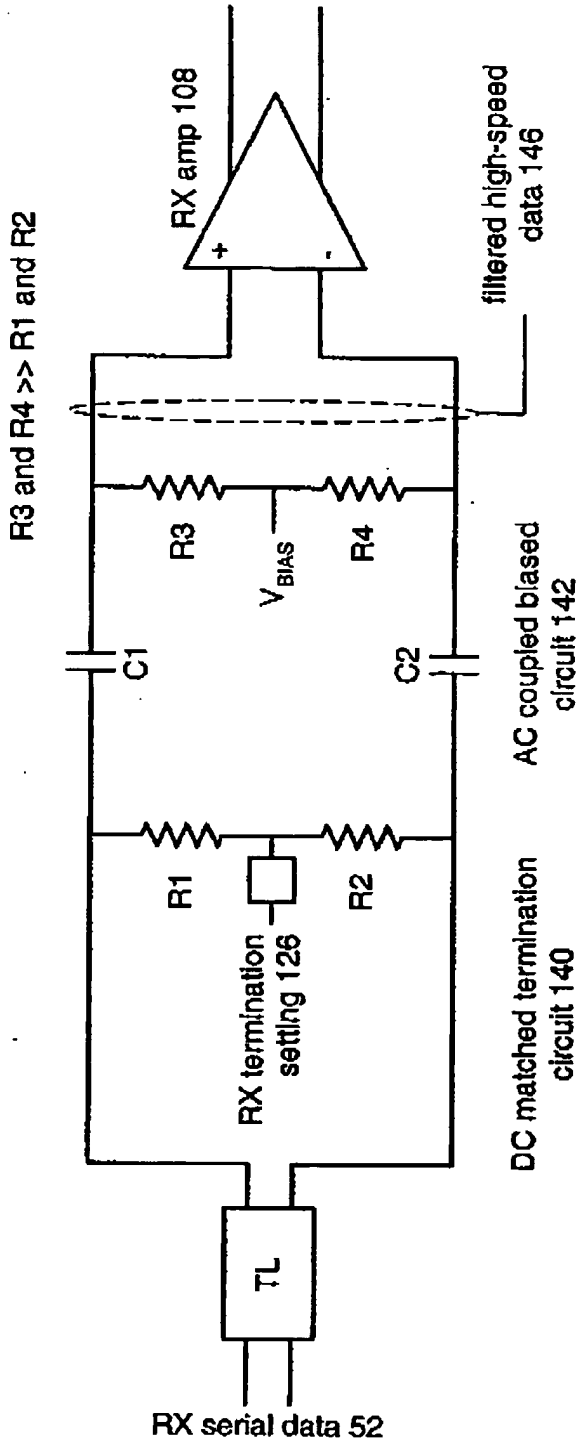

Figure 5

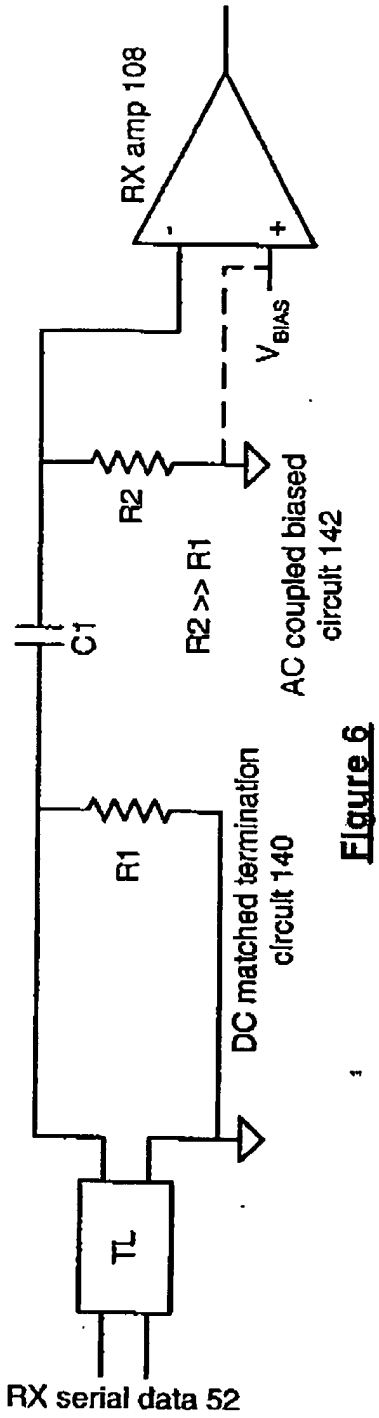

Figure 6

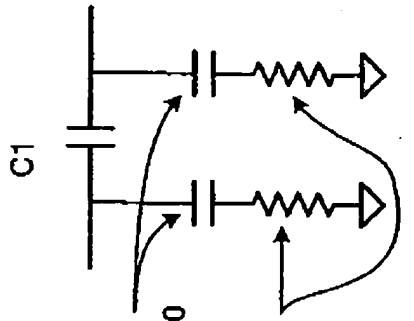

Figure 8
equivalent circuit of capacitor of Figure 7

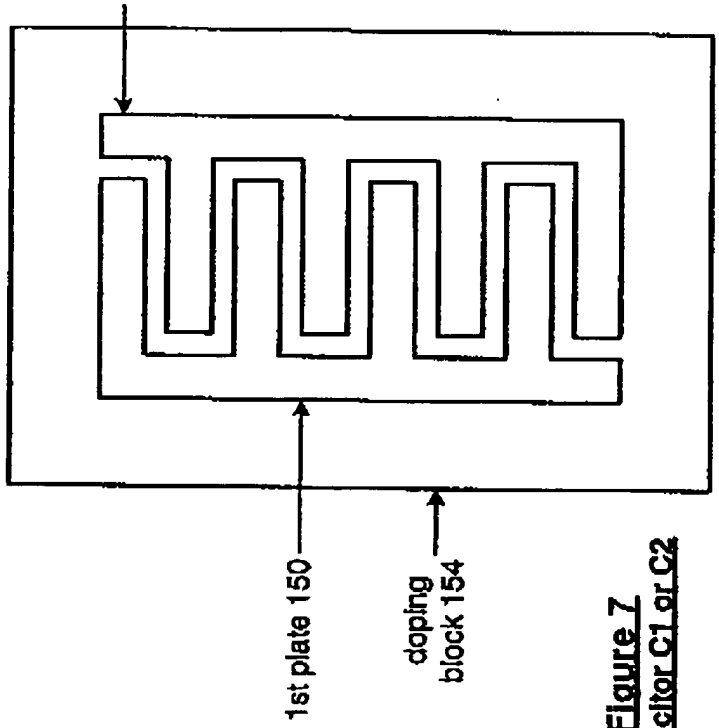

Figure 7
capacitor C1 or C2